EFFECT OF INTERMETALLIC COMPOUNDS ON THERMOMECHANICAL RELIABILITY OF LEAD-FREE SOLDER INTERCONNECTS FOR FLIP-CHIPS

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EFFECT OF INTERMETALLIC COMPOUNDS ON THERMOMECHANICAL RELIABILITY OF LEAD-FREE SOLDER INTERCONNECTS FOR FLIP-CHIPS

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BGA: Ball grid array

CSP: Chip scale package

CTE: Coefficient of thermal expansion

ENIG: Electroless immersion Gold

FCOB: Flip-chip on board

FEA: Finite element analysis

FEG: Field emission gun

FR4: Flame retarded

HASL: Hot-air soldering level

HTS: High temperature storage

IC: Integrated circuit

IMC: Intermetallic compound

I/Os: Input/Outputs

OSP: Organic solderability preservative

PWB: Printed wiring board

RF: Radio frequency

SEM: Scanning electron microscope

SOP: System on a package

TC: Thermal cycling

TSM: Top surface metallurgy

UBM: Under-bump metallurgy

LIST OF SYMBOLS

Au: Gold

E: Modulus

N_f: Creep-fatigue life

N_p: Fatigue life

N_c: Creep life

G : Shear Modulus

γ_p : Plastic shear strain

ν : Poison's Ratio

α: CTE (Coefficient of Thermal Expansion)

Δ: Change in, or Range when used with Strain

SUMMARY

Georgia Tech's Packaging Research Center's vision of System on Package (SOP) requires that the ball grid array (BGA) package be eliminated and the integrated circuit (IC) directly assembled on the printed wiring board (PWB). Flip-Chip on board (FCOB) emerges as a viable solution which meets the industry requirements of (i) increased I/O, (ii) increased functionality and (iii) improved performance at lower costs. Nevertheless flip-chip on board (FCOB) reliability continues to be an important concern in electronic packaging industry. Moreover transition to Pb-free solder for interconnects and continuously shrinking geometries result in new modeling challenges. In addition, the integrity of the intermetallics (IMCs) at the interfaces of the solder/PWB and solder/die is one of the determinant factors in the reliability and continuity of electrical signals in flip-chip interconnects. Pb-free solder studies for the flip-chip assembly studies are limited and simplified so far, not fully incorporating the effect of intermetallics in the reliability. New modeling challenges involve many details, from geometry to material properties. A brittle IMC will lead to a fracture at the interface. Also IMC thickness can cause the variation in stresses in the underlying layers, causing delamination. Moreover IMC morphology can also depend on the metal finishes on the PWB.

In this work, a combined numerical and experimental program has been developed to address the challenges mentioned above. The flip-chip on board assembly is modeled in 3-D for reliability studies, taking into consideration material non linearities and a 10^4 order of geometric variation to capture the die size in mm to sub-micron intermetallic thickness. The study intends to determine the stresses induced at the critical

interfaces under thermo-mechanical loading incorporating the intermetallic material properties. Various failure modes of these assemblies were studied.

Experiments were carried out for comparative reliability studies of Pb-free solder with eutectic Pb-based solder. Intermetallic formation and growth are characterized during thermal aging and its effect on reliability is determined. Parameters affecting intermetallic like under-bump Metallurgy (UBM) thicknesses are varied and its effect evaluated. Moreover experiments with three new substrate pad finishes on PWB are carried out to evaluate them as an alternative to Electroless nickel immersion gold (ENIG) for new Pb-free solder. The final aim of this study is to reach a better understanding of the reliability issues in FCOB.

CHAPTER 1

INTRODUCTION

This chapter introduces the subject of flip-chip. It briefly reviews the barriers to flip-chip technology particularly as the flip-chip interconnection is changed from lead-based to lead-free. One of these barriers is the formation of intermetallics and their effect on reliability. This forms the basis of the research proposed.

It begins by introducing the assembled flip-chip package and its various subcomponents. Next, the challenges created due to the transition to Pb-free solder in flip-chips are discussed. Further, the critical parameters affecting intermetallic formation in the flip-chip are identified. Thermo-mechanical reliability and intermetallics are discussed. Finally based on the challenges the objectives are listed.

1.1 Flip-chip in electronic packaging

Flip-chip microelectronic assembly is the direct electrical and mechanical connection of face-down (hence, functional side face down) bare die onto a package or printed wired board (PWB), by means of solder bumps typically deposited on the integrated circuit or wafer and bonded to the package or the PWB. A typical flip-chip on board (FCOB) is shown in Figure 1.1. The entire interconnection system can be subdivided into four functional areas under-bump metallization (UBM); encapsulation (underfill), solder ball and substrate pad with substrate pad finish or top surface metallurgy (TSM). UBM provides adhesion and acts as a barrier between the solder alloy

and the conductor metallization on the chip, such as Al or Cu. It consists of 3-4 different metal layers as shown in Figure 1.1(b).

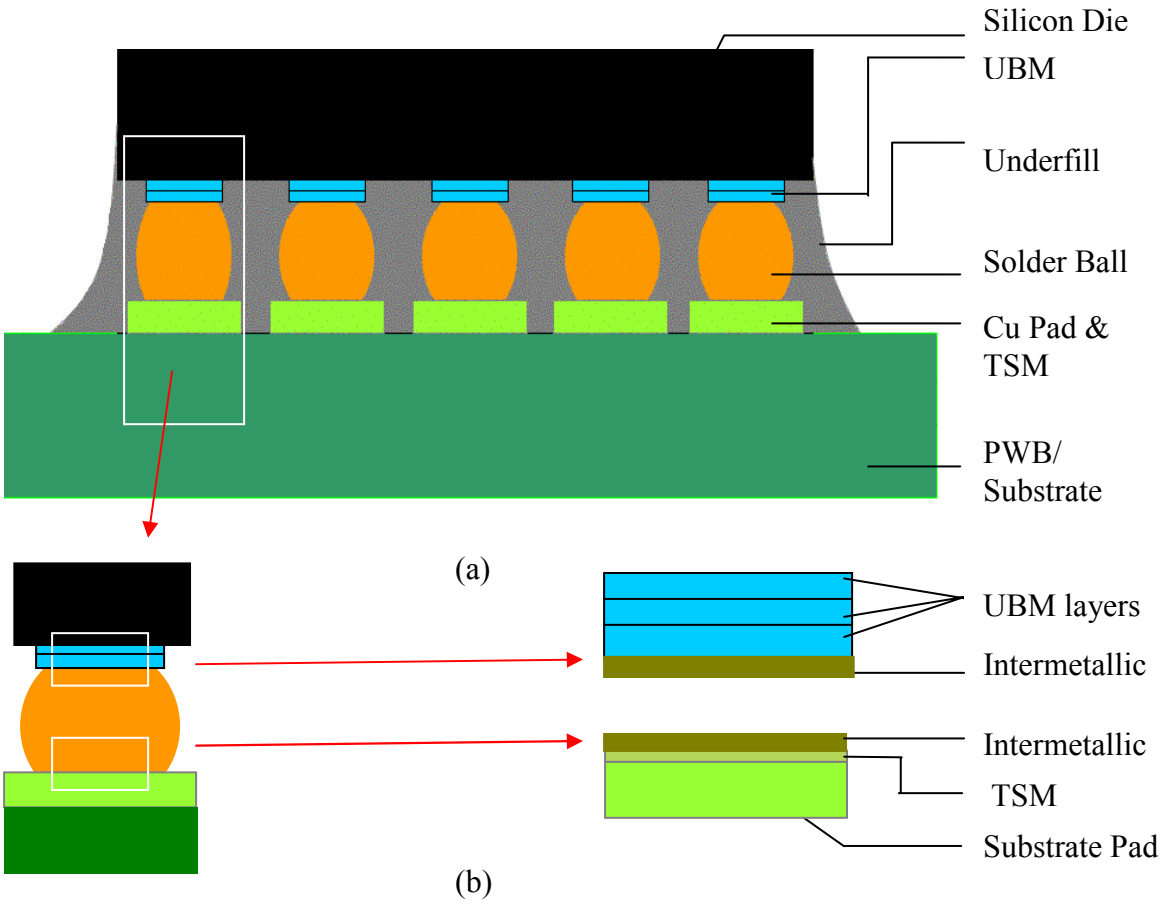


Figure 1.1 Flip-chip on Board. (a) Cross Section (b) Enlarged view of die/solder and solder/PWB interface

Underfill effectively binds the PWB with the die and distributes the stress in the solder joints. The origin of these stresses is discussed in Section 1.5. The solder ball/bump acts as the mechanical and the electrical connection from the silicon die to the PWB. The substrate pad (Cu) together with the TSM (different metal layers, usually Ni/Au) provides the interface between the solder and the PWB. During assembly, the solder melts and forms an intermetallic layer at the two interfaces as can be clearly seen

in Figure 1.1(a). This intermetallic layer at both the interfaces is extremely crucial for the overall reliability of the flip-chip.

Flip-chip package is very small and has a short signal path because of the small size of the solder bumps and also because the functional side of the die faces the substrate. It offers advantages in terms of performance, cost, volume and batch manufacturing.

1.2 Pb-free solder and flip-chip on board

The traditional solder bump in flip-chip is a Pb-based alloy (eutectic Sn/Pb or high Pb alloy), but Pb poses an environmental threat because of the improper disposal of old and obsolete electronics. Discarded PWBs can wind up buried in landfills, where lead oxides from the solder can become soluble, then leach into and contaminate groundwater. The movement towards complete lead-free product development is getting stronger. After the lead-free roadmaps developed by JEIDA, the Japanese Electronics Industries Association (1998) and NEMI, the National Electronics Manufacturing Initiative (1999), European Union published directives 2002/95/EC in January 2003, restricting the use of certain hazardous substances in electrical and electronic equipment (RoHS) by July 2006. Pb-free solders recommended as the most promising candidates by the National Center for the Manufacturing Sciences (NCMS) and the National Electronics Manufacturing Initiative (NEMI) are Sn3.9Ag0.6Cu (+/- 0.2%) for reflow soldering and Sn0.7Cu for wave solder. This change to Pb-free solder creates new challenges in assembly and reliability evaluation of the flip-chip. Since, Pb-free solders have higher melting points (217-221 ^{o}C) then the traditional eutectic Sn/Pb solder

(183 ^{o}C) and hence they require higher reflow temperatures during assembly (250-260 ^{o}C). This can lead to higher thermo-mechanical stresses and strains leading to reliability issues like PWB warpage, delamination of interfaces, fracture etc.

1.3 Assembly and intermetallic formation

The intermetallic forms during the assembly of the flip-chip on the PWB as is described in following paragraph. On the chip side, the typical UBM structure consists of three layers (1) **adhesion layer** such as Al or Ti/Cr , (2**) barrier layer** such as Ni and (3) **wetting layer** such as Cu or Au. During the assembly the wetting layer is dissolved completely and an IMC is formed. The intermetallic compound forms due to the dissolution of the **UBM wetting layer** into the molten solder during the reflow.

A typical TSM consists of two layers (1) the solderable layer touching the Cu pad and (2) the protective layer over the solderable layer. The purpose of the solderable layer is to provide the surface to which the molten solder will wet and then subsequently adhere on solidification. This solderable layer also prevents the diffusion of the solder to the substrate side base Cu pad. The protective layer, as the terminology implies, protects the solderability of the underlying solderable layer surface from being degraded by exposure to the ambient environment until the actual reflow occurs. During the reflow the solder melts and flows over the PWB pad. During this flowing, the protective layer dissolves and diffuses into the bulk of the solder. The underlying solderable layer is now exposed. Once exposed to the molten solder, the solderable finish is also subjected to dissolution by the molten solder until solidification has occurred. Thus an intermetallic is formed at the interface of solderable finish (the undissolved part) and the solder.

TSM serves two purposes. The first is to make the underlying Cu pad solderable. Besides solderability, TSM also acts as a barrier layer between the solder and the underlying substrate side pad material (Cu pad).

During subsequent aging after the assembly, the intermetallic layers on the substrate side can grow due to solid/solid reaction between the underlying solderability layer and the solid solder. IMC formed on the chip side can grow due to the solid/solid reaction between and the wetting layer (Cu) and the solid solder. The intermetallic formation and growth is shown in Figure 1.2.

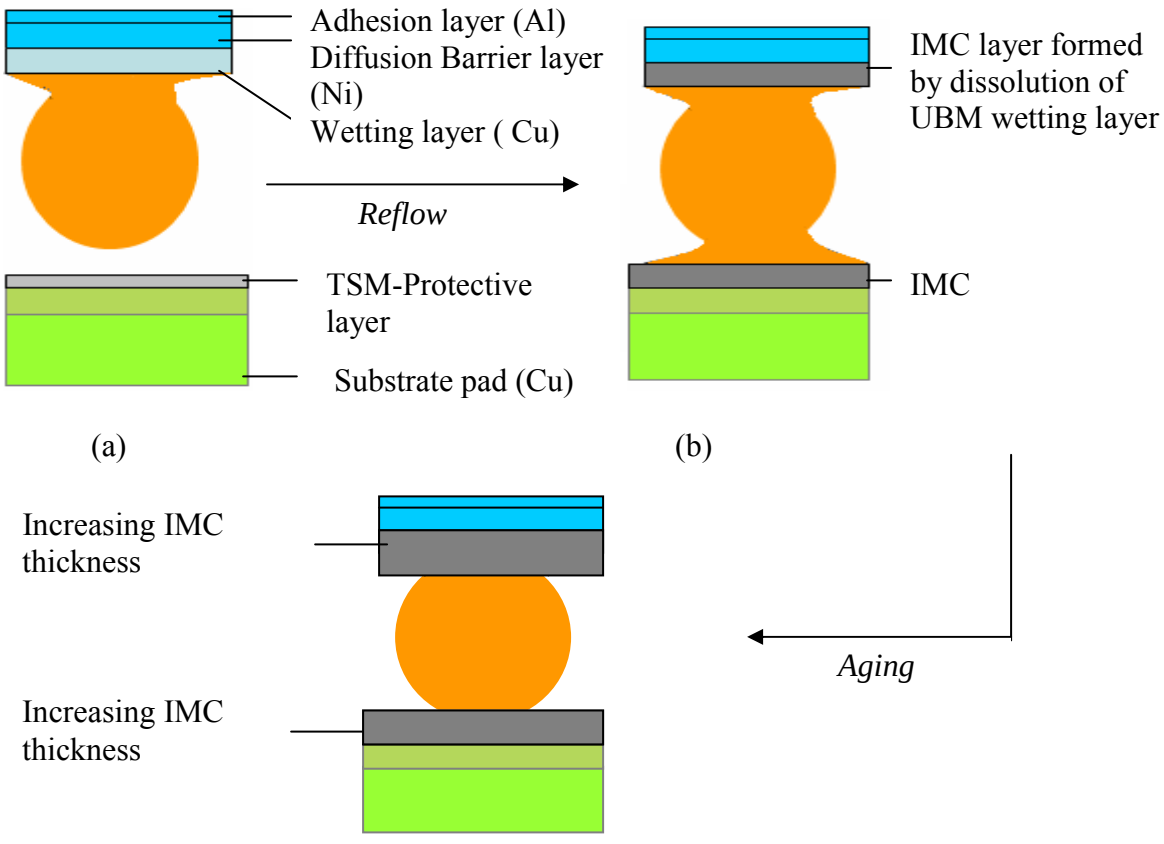


Figure 1.2 IMC formation in assembly of flip-chip. (a) Unassembled UBM and TSM (b) Reflowed assembled chip (c) Aged assembled chip

The intermetallic morphology, thickness etc depends on the solder composition, reflow temperature, duration and the substrate pad finishes.

The new Pb–free solder (Sn95.5-Ag3.8-Cu0.7) does not work well with current set of substrate pad finishes as the intermetallic reaction between copper and tin is particularly rapid [Korhonen et al., 2000]

- The growth of tin-copper intermetallics has been reported for leads covered with Pb-Sn eutectic solder. However, it is this same tendency of tin to form intermetallics that raises a long term reliability concern with high tin solders.
- Thus there is a need to explore the assembly and the reliability of the Pb-free bumped flip-chip with the newer substrate pad finishes of the PWB's. One of the research aims is the reliability assessment of different TSM's.

1.4 Increasing I/O's in flip-chip

Although flip-chip technology can achieve a far greater number of I/O than any of the currently available options, still increasing functionality and decreasing consumer electronic sizes demand for ever increasing I/O's. Table 1.1 show the ITRS projection to meet the requirements of increased functionality and higher speed integrated into a smaller volume. ICs are projected to push to nano-scale lithography (35 nm by 2014) and the number of I/Os are projected to cross 10,000 I/Os with a required pitch (distance between two solder bumps) of 30 to 70 μm.

Typically the solder ball height is half the pitch of the substrate pads. Increasing I/O's imply decreasing pitch size and eventually decreasing height of the solder bumps as well. This means that the percentage of intermetallic in the joint would increase. Besides as the surface pad finish differs from that of the molten solder, then the pad finish becomes, in fact, a contaminant to the solder in the joint. As the surface pad finish becomes thicker relative to the quantity of solder comprising the solder joint volume, it will have a greater effect on the composition; and therefore, on the properties of the solder once the wetting element from the pad finish has dissolved. The compositional change can cause an increase in the solder's liquidus temperature, resulting in premature solidification of the solder before the joint is completely formed. Contaminants may also decrease the solidus temperature of the solder, thus reducing the maximum service temperature to which the joint can be exposed. High contamination levels can lead to reductions in the mechanical strength and ductility properties of the solder after solidification (e.g. Au embrittlement). These problems can be particularly acute for fine-pitched solder joints. The small quantities of solder will experience higher contamination levels from the dissolved layer(s), resulting in a greater effect on their properties and that of the joint, before and after solidification. Thus different intermetallics growth and morphologies are studied for Pb-free solder vis-à-vis eutectic Pb –solder.

Table 1.1 Projection of key features of microsystems packages [*Source: ITRS*]

Technology Node years	**2005**	**2008**	**2011**	**2016**
Number of I/Os	3158	4437	6234	8758
Flip-chip pitch (µm)	130	90	80	70
Pad Size (µm)	65	45	40	35

1.5 Flip-Chip thermo-mechanical reliability

Thermo-mechanical failures are caused by stresses and strains generated within an electronic package due to thermal loading from the environment or internal heating during service operation or due to mismatch in coefficient of thermal expansion. Because flame retarded (FR4), the most common organic PWB material in use today has a fairly high coefficient of thermal expansion (CTE) compared with silicon, when the chip heats up through the electronic operation or environment, the PWB will heat up and expand a great deal more than the silicon. When the temperature decreases, through environment or cessation of operation, the PWB will contract. This introduces the shear strain in the solder joint. These shear strains cause shear stresses. High shear stresses can cause delamination of the various interfaces like UBM /intermetallic, solder/underfill etc. The new Pb-free solder not only has thicker and brittle intermetallics but experiences higher reflow temperatures causing higher stresses at the joints. These not only cause delamination but also fatigue of the solder joint if the repeated cooling and heating of the assembly takes place. This effect is similar to bending a paper clip back and forth. Lead-free solder joints will fail due to low cycle fatigue from the CTE mismatch. The high shear stresses would enhance the fatigue initiation. Hence evaluation of stresses at the joints becomes critical to predict the reliability of the assembly.

Also, lower plastic shear strain or higher height of the solder bump would favor longer solder joint fatigue life. As discussed in Ssection 1.2 increasing I/0's leads to decreasing solder bump height of the bumps, causing faster fatigue initiation and failure.

Thus increasing shear stresses undermines thermo-mechanical reliability. But how much does the stress get affected by the presence of intermetallics in an ever decreasing

bump height remains to be explored. This can be understood by changing the UBM wetting layer thickness and creating a FEM model which takes into account the intermetallic thickness and the material properties. This research aims at accomplishing the same.

1.6 Objectives of research

Based on the challenges discussed above, this research endeavors at understanding the thermo-mechanical reliability of Pb-free solder flip-chips as affected by the intermetallics on both the chip/solder and the solder/substrate side. It addresses the affect of different substrate pad finishes and different UBM thicknesses on the reliability. Specifically, this work aims to attend to the following questions:

- How does the intermetallics affect the flip-chip reliability of Pb-free solder (SnAgCu) vis-à-vis eutectic solder?
- How does changing UBM wetting layer thickness (or intermetallic thickness) affect the stress variation at the joints for Pb-free solder during reflow and subsequent thermal cycling ?
- How does various substrate pad finishes perform with different Pb-free solder?

In order to address these issues high temperature storage (HTS), Thermal shock, Ball shear, die shear, SEM/EDX have been conducted. Experimental results have been supported by finite element analysis (FEA) results and these results are discussed in detail.

1.7 Thesis organization

This section describes the organization of the rest of the chapters in this thesis and how the research goals have been broken down. Chapter 2 gives a comprehensive overview of the existing literature and background related to this research. Chapter 3 discusses the finite element modeling (FEM) developed including the material properties used. Chapter 4 discusses the results from the FEM model for different UBM thicknesses. It estimates the stress variation in the critical regions and discusses the potential failure mechanisms in the assembly, namely delamination of the critical interfaces and solder joint fatigue. Chapter 5 describes in detail the various experimental methods employed in this research. Pb-free solder is compared with Pb- based solder and various parameters affecting the reliability are studied. A discussion on intermetallics is also provided. The last chapter; Chapter 6 provides a brief summary of the work and states the recommendations for future work.

CHAPTER 2

BACKGROUND AND LITERATURE SURVEY

This chapter provides background information relevant to the various substrate pad finishes and UBM's. It aims to bolster the case to explore new pad finish materials for Pb-free solder and to develop a comprehensive model for failure analysis of the FCOB. It starts with a short survey of the various substrate pad finishes being used in boards finishes, including disadvantages and advantages of each. A brief overview of the current UBM technologies being used in flip-chips is discussed. This is followed by a discussion of various failure mechanisms in flip-chip assemblies at interfaces and solder.

2.1 Top surface metallurgy (TSM) or substrate pad finishes

This section gives a brief survey of the different substrate pad finishes on the Cu pad of the FR4 substrate. The four different pad finishes commonly used are Hot-air solder leveling (HASL), Organic solderability preservative (OSP), Electroless nickel immersion gold (ENIG) and Immersion silver.

2.1.1 Hot-air solder leveling (HASL)

Hot air solder leveling is the solder coating over bare PWB. The circuit board is coated with flux and then immersed into the bath of molten solder. The board is then withdrawn and immediately passed between two hot air jets which blows away excess molten solder from the pads. A thin, coating of solder is left on the exposed, conductive features as shown in Figure 2.1. HASL provides excellent solderability protection of the

underlying surface because the films are 100 percent dense. Another advantage of the hot-solder dipping process is that any solder composition can be applied to the part. This is an advantage as compared to the case of electroplated or electroless coatings (Section 2.1.3) in which the finished composition is limited to available bath chemistries, which do not represent the wide range of available solder compositions. The biggest disadvantage with HASL is its inability to produce planar and uniform coating. Hence for fine pitch applications their utility is limited.

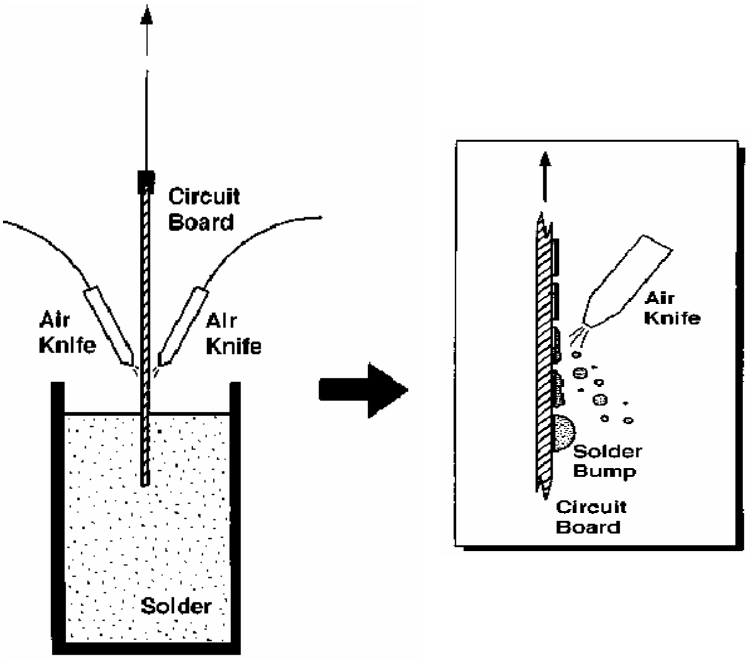


Figure 2.1 HASL coating

2.1.2 Organic solderability preservative (OSP)

Organic solderability preservatives, or OSP's, are an important group of protective finishes for bare Cu. Three classes of organic compounds are currently used by

the electronics industry as OSPs namely benzotirazole compounds, imidazole compounds and benzimidazole compounds. Figure 2.2 shows the OSP coating.

These compounds protect the Cu surface by actually forming a chemical bond with the Cu that prevents the latter's oxidation. With respect to solder processing, the OSP coating functions by protecting the Cu surface up to the start of the soldering process.

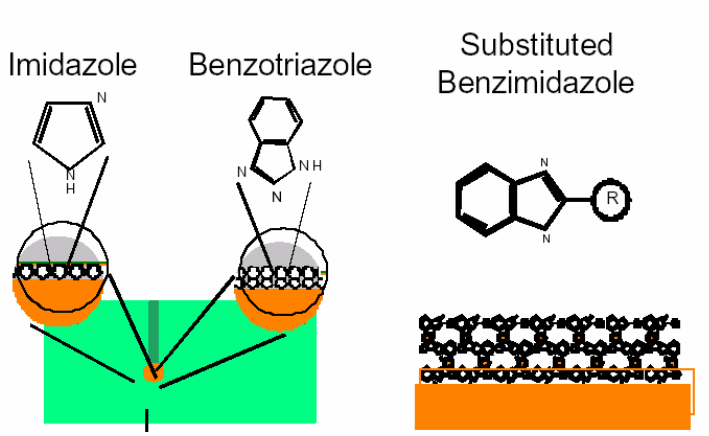


Figure 2.2 OSP coating.

During soldering, the elevated temperatures (typically 120°C to 150°C) cause the OSP coating to dissipate into the furnace environment, thereby exposing the Cu surface to the flux and environment followed by wetting and spreading of the molten solder. In the event that the OSP coated Cu is exposed to a process cycle in the absence of flux and solder, the coating is lost as described. In general, solderability protection improves significantly when OSP coating are used in conjunction with N_2 atmosphere during the soldering process.

OSP provides very flat solder pad surfaces and excellent compatibility for consistent and uniform solder paste application for fine pitch application. But very careful material handling procedures must be followed. Human salts are capable of degrading the coating such that the solderability of the copper will be compromised. OSP finished printed circuit boards may not be suitable for radio frequency (RF) circuitry assemblies. Most RF boards require a metal shield to be soldered and in contact to the grounding trace, thus providing the necessary shielding. The organic coating and the shield may not provide sufficient grounding trace.

2.1.3 Electroless nickel immersion gold (ENIG)

Electroless nickel (Ni) layer is added between the Copper (Cu) and the Gold (Au) layer. The Au layer is the protective finish, and is dissolved by the molten solder as it wets and spreads over the part. The final wetting by the molten solder is to the Ni layer.

The Ni typically deposited is from Ni-Phosphorous (P) solution by electroless plating. During exposures to high temperatures, P migrates to the interfaces. This reduces the ductility and hence can potentially induce loss of solder joint. Therefore lower Phosphorous bath chemistries (6 %) are preferred. The 6 to 10 mil immersion gold thickness plated deposition protects the underlying nickel-plated coating from oxidization. During reflow the gold dissolves into the tin/lead solder. The actual solder joint intermetallic is tin and nickel.

Au is deposited by immersion process which is basically the galvanic displacement reaction. Au displaces some of the Cu from the Cu pad and forms a flash layer. Electroless nickel immersion gold (ENIG) provides very flat solder pad surfaces

and excellent compatibility for consistent and uniform solder paste application. PWB handling is not as sensitive as it is for the OSP finishes. ENIG plated boards can be used for nearly all kinds of electronic assembly applications including RF.

One of the problems is known as “black pads.” “Black pads” result in defects, and weak inferior solder joints. “Black pad” is formed at random on certain solder pads by corrosion of the nickel in the immersion gold process. This might result in the crack at the Ni and Cu interface.

2.1.4 Immersion silver

Immersion silver is deposited by a galvanic exchange reaction where Ag displaces the Cu of the pad.

$Cu\ (metal) + a\ Ag^{+} \rightarrow 2Ag\ (metal) + Cu^{2+}$

Immersion silver is suitable for thin board production down to 4 mils. It is flat and has uniform thickness. It maintains solderability with a long shelf life.

It has low temperature process and eliminates thermal shock. It can also be used very well with lead-free chemistry. One important disadvantage is that silver gets tarnished in presence of sulphur and chlorine from atmosphere; hence special packaging requirements are needed.

2.2 Under-bump metallization (UBM) in flip-chips

As discussed in Chapter 1, the thin film UBM consists of multi metal layers. It should be robust enough to resist several number of flows (wetting reaction) for assembly and long periods of thermal aging (solid state diffusion) during service. The integrity of thin-film UBM is therefore crucial to the reliability of flip-chip packages. For this

research, several potential UBM schemes were overviewed before selecting the one with best known performance in terms of reliability for FCOB. But even for a defined set of material layers the thickness of each layer in UBM is important as it controls diffusion or IMC formation. In this research the wetting layer thickness is varied in order to understand the effect of IMC thickness formation on the FCOB reliability.

2.2.1 Alternative UBM schemes

While the industry is moving towards Pb-free production, there are challenges encountered in elucidating an appropriate UBM system for flip-chip interconnections. The Pb-free solder candidates such as SnAg and SnAgCu, usually contain a higher percentage of Sn and causes higher reflow temperatures and severe interfacial reactions between solder and UBM [Zhang et al., 2002]. The conventional Cr/CrCu/Cu based UBM is found to no longer be compatible because of the fast spalling of intermetallic from the interface.

Ni based UBM, thus emerged mainly because of the slow reaction rate between Sn and Ni [Kim et al., 1995 ; Rai et al., 1995 ; Jang et al., 1999]. Hansen and associates [Hansen et al., 1985] reported that this can be explained by the phase diagrams of the materials involved. From the binary phase diagrams, not only Cu, Cr are immiscible [Hansen et al, 1985] but also Sn and Cr. Therefore, we expect Cu-Sn compounds to have a weak interaction with Cr. And so the spalling of Cu_6Sn_5 IMC with the Cr/CrCu/Cu UBM occurs [7]. In contrast Cu, Ni and Sn, Ni are miscible, and therefore Cu_6Sn_5 and Ni have a low energy interface and hence the intermetallics are not expected to spall. Thus getting a low energy interface is the key, which depends on how well the miscibility is.

Even among Ni based UBM's, Al/Ni(V)/Cu UBM has attracted more and more interest recently [Liu et al., 2000]. In this UBM system, Cu acts as a wetting layer to the solder and Ni as a diffusion barrier. It needs to be mentioned that V is co-sputtered with Ni during the process to mitigate the magnetic interference of Ni and to speed up the sputtering [Hansen et al.].

Though literature describes stress generation in the Ni metallization during the UBM deposition but lacks understanding for the same during thermo-mechanical reliability testing. Korhonen TM, Su P, Hong SJ, Korhonen MA, Li CY reports that although stresses increase somewhat with Ni content ; the adhesion layer under the CuNi layer has a much larger effect on the stress [Korhonen et al., 2000]. The Ni containing metallizations tend to have higher stresses that may lead to peeling of the metallization or failure of the joint. The residual stresses are believed to be associated with the columnar grain structure and/or lattice defects forming during film deposition. Subsequent relaxation of grain boundary structure and other lattice defects leads to densification of films such that the films are put in tension and the wafer in compression.

The stress generation in the UBM due to the intermetallic layer formation during thermo mechanical reliability can give a clue about possibility of the delamination or crack initiation in the UBM. This delamination can lead to fracture or an electrical open. This stress generation will vary with the IMC thickness formed, which again depends on the initial wetting layer thickness (Cu). Hence a model that correlates the IMC thickness to the stresses in the underlying Ni metallization is necessary.

2.3 Thermo-mechanical failure modes

Thermo-mechanical failures are caused by stresses and strains generated within an electronic package, causing the package to fail in a variety of ways as discussed in Section 1.5. The modes of failure that are common in FCOB and chip scale packages (CSP's) are failure of the silicon IC due to cracking, delamination of various material interfaces, and fatigue cracking of the solder. [Ewell et al. 1998]

2.3.1 Delamination at interfaces

Delamination is the bonding of adjacent layers of different materials which were bonded before. The presence of delamination can affect the reliability of the package. For example, in the multilayered structures, the delamination may cause electrical open. Delamination initiates due to high interfacial stresses.

There are no clear criteria to predict the initiation of delamination. One approach is to determine the interfacial shearing and peeling or opening stress as shown in Figure 2.3 [Tummala, 2001] and make a comparison with the interfacial shear strength (τ_{yx}) and peel strength (σ_{yy}). Tummala [Tummala, 2001] sites that delamination is expected to initiate, when the following equation is true:

$$\frac{\Gamma_{yx}}{\Gamma_{\text{exp, yx}}} + \frac{\sigma_{yy}}{\sigma_{\text{exp, zz}}} \geq 1$$

where $\tau_{\text{exp,yx}}$ and $\sigma_{\text{exp,yy}}$ are the experimental shear and peel strengths.

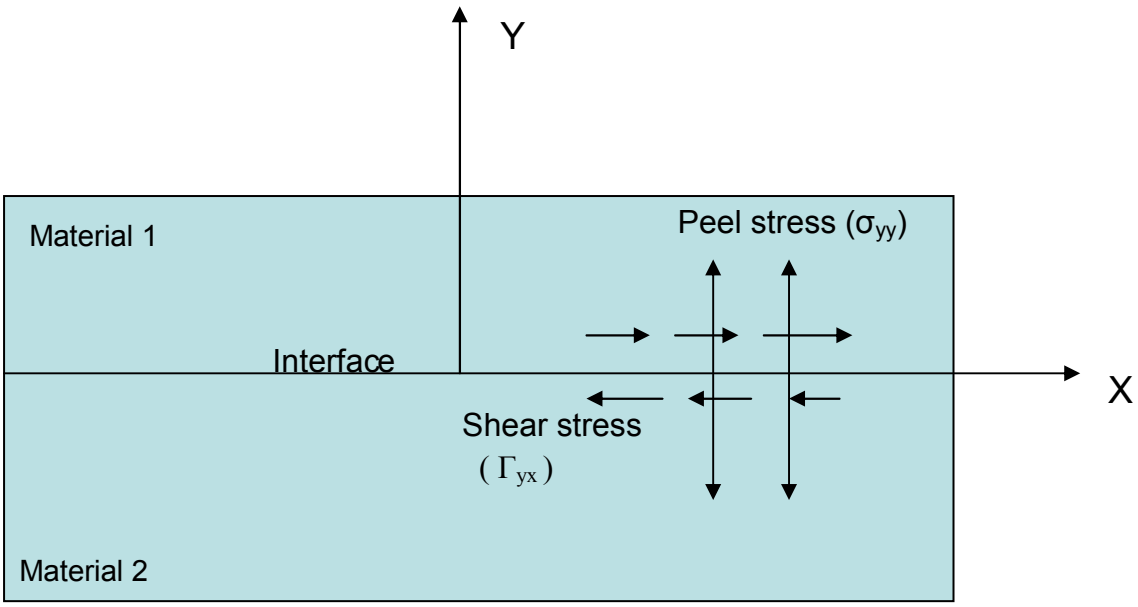


Figure 2.3 Schematic of interfacial stresses.

The above model is a simplified, two dimensional model whereas the actual FCOB assembly is a 3-D geometry with various interfaces under high stresses. In order to identify the potential delamination sites, a 3-D FEM model is needed which takes into account the various UBM metal layers as well as the IMC formation.

2.3.2 Solder joint fatigue

When area array packages with solder connection are thermally cycled, the inelastic material characteristics of the solder contribute to increasing amounts of strain. This inelastic strain increases consistently with every thermal cycle, and experimental relationships have been established that relate this cyclical strain rate to the number of cycles that the solder connection works. The first step in using these relationships is calculating the inelastic shear strains that accumulate over a single thermal cycle. The

equivalent plastic strain over a single load step during a temperature cycle can be calculated form the change in component strains as:

$$\Delta\varepsilon_{eqv}^{p} = \frac{\sqrt{2}}{3}\sqrt{\left(\Delta\varepsilon_{x}^{p} - \Delta\varepsilon_{y}^{p}\right)^{2} + \left(\Delta\varepsilon_{y}^{p} - \Delta\varepsilon_{z}^{p}\right)^{2} + \left(\Delta\varepsilon_{z}^{p} - \Delta\varepsilon_{x}^{p}\right)^{2} + \Delta\gamma^{p}}$$

$$\Delta\gamma^{p} = \frac{3}{2}\left(\Delta\gamma_{xy}^{p^{2}} + \Delta\gamma_{yz}^{p^{2}} + \Delta\gamma_{zx}^{2}\right)$$

The equivalent plastic strain from each load step can then be summed up to calculate effective plastic strain over one cycle:

$$\varepsilon_{eqa}^{pl} = \sum \Delta\varepsilon_{eqa}^{p}$$

Plastic shear strain range in the Coffin-Manson type formulations and can be calculated from the effective plastic strain as [Zheng et al., 1994]

$$\Delta\gamma_{p} = \frac{\sqrt{3}}{2}\varepsilon_{eqa}^{pl}$$

Cyclical plastic shear strain can be related to fatigue life in a Coffin-Manson type relationship.

$$N_p = a\ \Delta\gamma_{p}^{-n}$$

Where the constant *n* and *p* are material properties evaluated via experiments. Modified Coffin-mansion equations can then be used to determine the mean number of cycles to failures based on the equivalent strain rates [Michealides and Sitaraman, 1998 & Hong and Su, 1998]

2.4 Summary

A brief survey of the various substrate pad finishes in boards and UBM metallizations in flip-chips has been presented in this chapter. None of the current pad finishes has been explored extensively for the new Pb-free solder based assembly. In order to understand the reliability needs of the new Pb-free flip-chip, a comparative study is needed vis-à-vis Pb-free solders and Pb-based solder which takes into account IMC formation. Also, due to the mismatch in properties among different materials in flip-chip assemblies, thermally induced stresses and strains are generated that could lead to failure of the assembly. A further trend of changing the UBM wetting layer thickness may lead to delamination of the underlying layers. Besides other failure modes are also present in the FCOB assembly, which are related directly or indirectly to the IMC thickness. Hence comprehensive analytical models that relate IMC thickness to the overall thermo-mechanical reliability of the package is needed

There is also a need to experimentally study the reliability of the new Pb-free solder and Pb-based solder. The effect of changing UBM thickness and pad finish of the board on overall reliability and performance of the package has not yet been addressed completely.

CHAPTER 3

FINITE ELEMENT MODELING

This chapter describes the developed FEA model. It starts with the need for the global/local approach. This is followed by the various material models used including Pb-free solder. Subsequently the loading conditions are described.

3.1 Modeling overview

3.1.1 Geometry

The geometry of the flip-chip on board has a first order effect on the reliability of the package. That is to say, changing the parameters involved in the geometry of the package directly affect the reliability. Solder pitch, standoff solder height, are only a few of the parameters involved in the construction and development of a model that can adequately characterize the geometry of the package. The order of magnitude involved in the geometry of a flip-chip varies from 10^4, from chip dimensions in mm to the sub- micron layer in the UBM and IMC thicknesses. In order to capture such a broad spectrum of dimensions, a unified approach to FEM modeling does not work well. Hence the problem is overcome by coarse modeling of the FCOB assembly. The results obtained from the coarse or global model are subsequently used to construct the most critical region in finer detail. This critical region is the submodel and is studied for failure mechanisms. This modeling approach results in global and local/cell model. Table 3.1

lists the thickness of the cross section that is used. The thickness values are captured from the SEM images of a cross section of an assembled FCOB.

Table 3.1 Parameters used in modeling

Geometry	Thickness (µm)
Die	525
FR4	625
Pitch	250
Solder Bump	125
UBM	*UBM-Al* = 0.4
	UBM-Ni = 0.32
	UBM-IMC = 0.6
Cu Pad	37.5
Pad Finish	*Ni of ENIG* = 4.5
	IMC formed = 2.52

3.1.2 Global model

The global model is a 3-D quarter symmetry model having 64 solder bumps. The geometry was created using bottom up approach, creating the substrate first, followed by the copper pad, solder interconnect, and the silicon die. Figure 3.1 shows the quarter symmetry model for flip-chip on board with the vertical rigid-body constraint at a corner node to prevent rigid body motion. Figure 3.2 shows the top view of the same quarter

symmetry 3D model with the x and y direction symmetry constraints. Parametric modeling was used to model the above geometry.

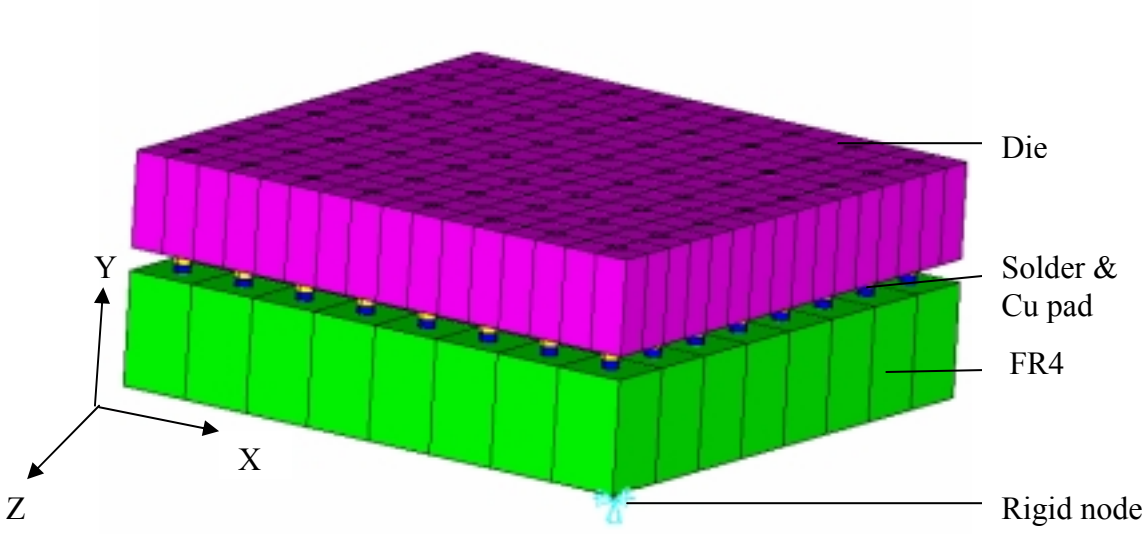


Figure 3.1 Quarter symmetry model of flip-chip on board.

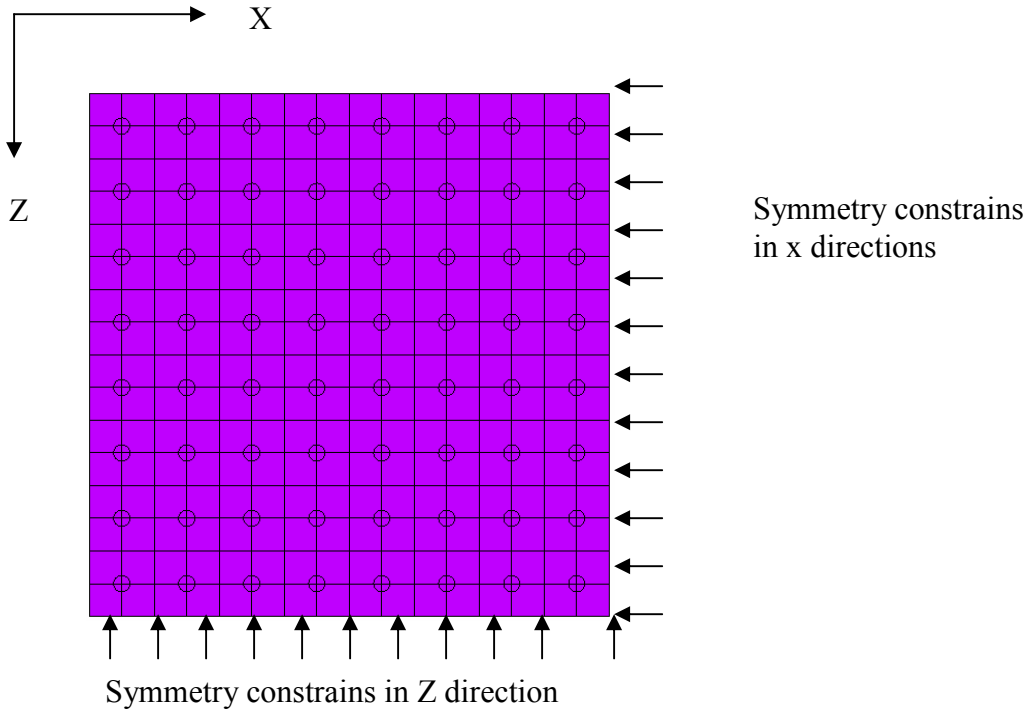


Figure 3.2 Top view of quarter symmetry model with constraints.

3.1.3 Local/Cell model

The local model was constructed for the solder joint experiencing the maximum strain. This was the corner most solder joint. This joint included sub-micron features like, UBM thicknesses, intermetallic thickness etc. The cross section of the geometry is shown in the Figure 3.4. The thickness of the pad_IMC is approximated from the SEM of the assembled flip-chip. Figure 3.3 shows the SEM image and average value of the pad_IMC as 2.52 μm for SnAgCu solder-pad interface. The boundary conditions for the local model are estimated from the interpolation of the global model based on St Venanat's Principle. The principle implies that stress concentration effects are localized around the concentration; therefore, if the boundaries of the submodel are far enough away from the stress concentration, reasonably accurate results can be calculated in the submodel. Appropriate care has to be taken so as to ensure that the boundary condition is sufficiently away from the region. The boundary conditions are shown in Figure 3.5.

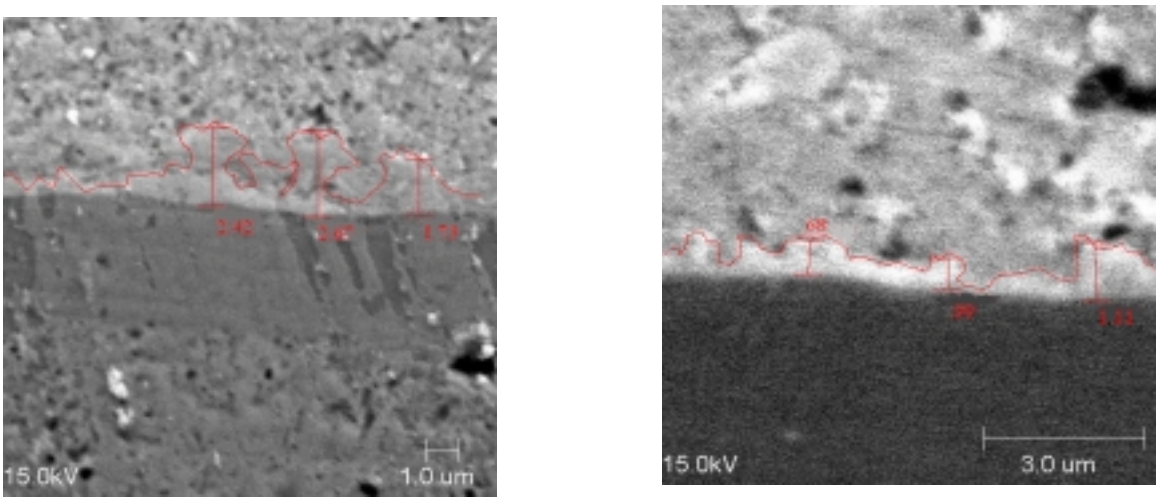
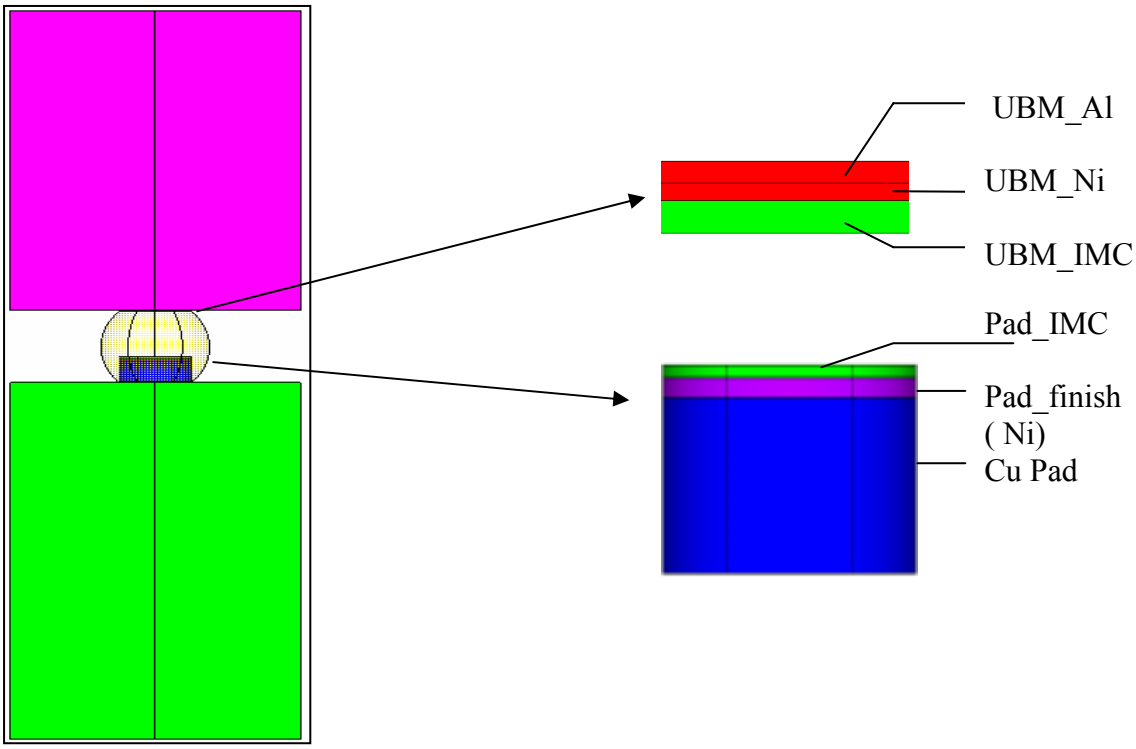


Figure 3.3 As reflowed pad_IMC thickness. (a) Sn3.8-Ag-95.5-Cu (b) Sn63-Pb37



(a) (b)

Figure 3.4 Cross-section of Cell/Local model. (a) Entire cross section (b) UBM/solder interface and FR4/solder interface

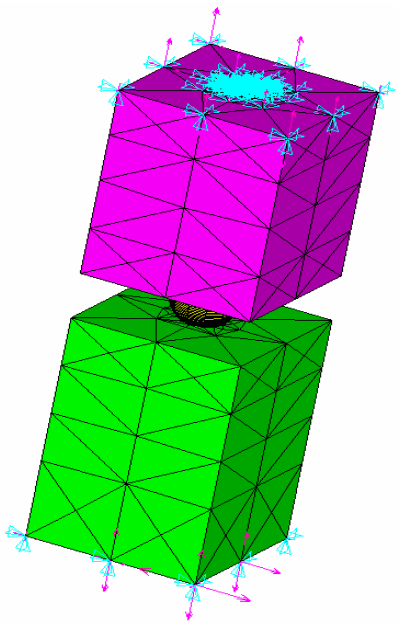


Figure 3.5 Boundary conditions of cell model (interpolated from the global model).

3.2 Material modeling

The constituent material modeling is presented and discussed. Depending on the failure mode studied, the material model(s) can have different degrees of sophistication. For example, in the case of backside die stresses and die cracking after assembly, the creep properties of solder need not be considered and this will have minimal effect on die stresses. In the case of solder fatigue, it is critical to consider the creep behavior of the solder material. Then again creep importance would depend on the homologous temperature of the solder. Lead-free solders have a higher melting point and hence it is expected that creep would be less than in Pb-free solders. It is important to note that when a material property is temperature dependent, and the value of the temperature dependent property is measured or known in a given temperature range, the numerical model interpolates the data within that range. The following sections describe the material modeling for the various components in the flip-chip assemblies.

3.2.1 Lead-free solder

Solder material exhibits complex behavior. Its mechanical properties depend on temperature, frequency, time, strain rate and even grain microstructure. Plasticity effects of solder are characterized by using the Multilinear Kinematic hardening model (MKIN). The silver-containing alloys exhibit much greater creep resistance, typically a hundred fold and a thousand fold for the binary and ternary, respectively. Thus creep is not modeled for the lead-free solder [Plumbridge et al., 2001].At present the entire spectrum of solder properties for a specific SnAgCu composition is not known with certainty. Hence mechanical properties for Sn95.5-Ag3.8-Cu0.7 and SnAg4Cu0.5 are used in

conjunction. Since these two alloys are very similar in composition. Moreover properties are extrapolated for the range -55C to 125C, from the limited temperature range for which the data is available.

Table 3.2 Multi-kinetic elastic plastic model for SnAg4Cu0.5 [Weise et al. , 2003]

SnAgCu [T]	**ε1**	**ε2**	**σ1[MPa]**	**σ2[MPa]**	**σ3[MPa]**
278	1.4E-3	4E-3	57.4	80	2500
323	1.4E-3	4E-3	53.2	72	1900

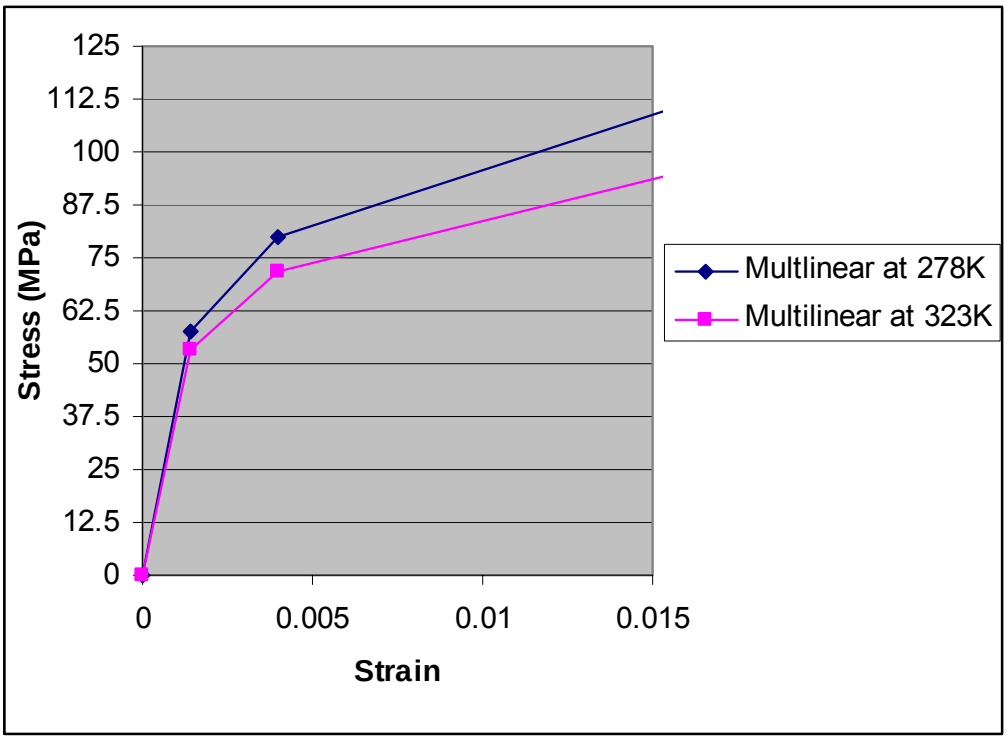


Figure 3.6 Stress strain behavior of SnAg4Cu0.5 solder plotted from Table 3.2.

Elastic modulus is modeled as linearly varying function of Temperature. It's parameters are obtained from the elastic region of the figure 3.4.

Y(T) = x + yT

41000 (278K) = x + y 278

38000 (323K) = x + y 323

Solving equation 1 and 2 we get:

Y(T) = 59533 -66.7*T

CTE is modeled as a Temperature varying function. Table 3.2 shows the average values of the CTE in the respective temperature regimes. These values are used to model the CTE as discussed below.

Table 3.3 Coefficients of thermal expansion for Sn95.5-Ag3.8-0.7Cu [Weise S. et al., 2001]

Temperature range	**Temperature range (K)**	**CTE**
20-100 ^{o}C	293-373	16.7
100-150 ^{o}C	373-423	18.8

CTE (T) = x +yT

$$16.7 = \frac{\int_{293}^{373}(x+yT)dT}{(373-293)} \quad \text{---------- 1}$$

$$18.8 = \frac{\int_{373}^{423}(x + yT)dt}{(423 - 373)} \quad \text{---------- 2}$$

Solving equation 1 and equation 2 for x and y we obtain the CTE of the lead-free solder as: CTE (T) = 14.761538 + 1.1834E-4*T

The poison's ratio used is 0.4.

3.2.2 FR4 (Substrate)

The FR4 boards consist of layers of glass and epoxy with copper layers, laminated together under high temperature and pressure to make a solid material. This manufacturing process makes the boards highly orthotropic. Below its glass transition temperature (T_g), the FR4 is in hard, glassy state. Above its T_g, the material becomes noticeably softer. Therefore FR4 is modeled as a temperature dependent, anisotropic material. Table 3.4 shows the material properties that were used for FR4. One must bear in mind, that for this simulation, the Y axis represents the thickness of the FR4, and the X and Z axes form a plane on the surface of the PWB.

Table 3.4 Thermal and mechanical properties of FR4 (CINDAS Database, 1995)

Material Property	**Value**
E (at 30 ^{o}C)	x) 242.64 MPa y) 15 MPa z) 242.64 MPa
E (at 95 ^{o}C)	x) 225.44 MPa y) 11.0 MPa z) 225.44 MPa
E (at 110 ^{o}C)	x) 211.64 MPa y) 9.0 MPa z) 211.64MPa

E (at 150 ^{o}C)	x) 197.84 MPa y) 5.0 MPa z) 197.84 MPa
E (at 270 ^{o}C)	x) 178.64 MPa y) 3.50 MPa z) 178.64 MPa
Poison's Ratio, ν	x) 0.1425 y) 0.1360 z) 0.1425
Shear Modulus, G	x) 199.0 KPa y) 630.0 KPa z) 199.0 KPa
CTE (at 30 ^{o}C)	x) 16 x 10^{-6} /^{o}C y) 57 x 10^{-6} /^{o}C z) 16 x 10^{-6} /^{o}C
CTE (at 95 ^{o}C)	x) 16 x 10^{-6} /^{o}C y) 57 x 10^{-6} /^{o}C z) 16 x 10^{-6} /^{o}C
CTE (at 125 ^{o}C)	x) 16 x 10^{-6} /^{o}C y) 235 x 10^{-6} /^{o}C z) 16 x 10^{-6} /^{o}C
CTE (at 150 ^{o}C)	x) 16 x 10^{-6} /^{o}C y) 235 x 10^{-6} /^{o}C z) 16 x 10^{-6} /^{o}C
CTE (at 270 ^{o}C)	x) 16 x 10^{-6} /^{o}C y) 235 x 10^{-6} /^{o}C z) 16 x 10^{-6} /^{o}C

3.2.3 Cu (Substrate pad)

The copper pads are formed on the PWB to bind to the solder joints. FR4 boards consist of layers of glass and epoxy with copper layers, pressed together under high temperature and pressure to make a solid material. These copper pads are modeled using bi kinetic isotropic (BKIN) temperature independent properties, because the properties of copper do not change significantly through the temperature range of -55^{0}C to 125^{0}C.

Table 3.5 Thermal and mechanical properties of copper (CINDAS Database, 1995)

Material Property	**Value**
Elastic Modulus, E	103.42 GPa
Poison's Ratio, ν	0.34
CTE, α	17 x 10^{-6} /^{o}C
Yield Strength	172.38 MPa
Tangent Modulus	1034.2 MPa

3.2.4 Ni (ENIG and UBM layer)

The Ni in the geometry arises in ENIG substrate pad finish and in UBM as diffusion barrier layer. The deposited Ni in the UBM contains only 7 % vanadium. Similarly Ni in ENIG contains 6-10 % P. We assume pure Ni in the ENIG and UBM and model that.

Table 3.6 Thermal and mechanical properties of Ni [Matweb and Metals Handbook]

Material Property	**Value**
Elastic Modulus, E	207000 MPa
Poison's Ratio, ν	0.31
CTE, α	13.1 x 10^{-6} /^{o}C
Yield Strength	317.0 MPa
Tangent Modulus	1034.2 MPa

3.2.5 Cu_6Sn_5 (Intermetallic)

The intermetallic is modeled as a layer of Cu_6Sn_5 . Although other intermetallics might evolve during thermal storage and thermal cycling testing, the predominant layer is assumed to be Cu_6Sn_5. Hence we use Cu_6Sn_5 material properties for IMC modeling.

Table 3.7 Thermal and mechanical properties of Cu_6Sn_5 [Frear et al., 1994 and Fields]

Material Property	**Value**
Elastic Modulus, E	85.56 GPa
Poison's Ratio, ν	0.309
CTE, α	16.3 x 10^{-6} /^{o}C
Fracture Toughness (KIC)	1.4 MPam$^{-1/2}$

3.2.6 Aluminum (UBM adhesion layer)

The Al properties are as described in Table 3.8.

Table 3.8 Thermal and mechanical properties of Al [Alok Nayer, 1997].

Material Property	**Value**
Elastic Modulus, E	68 GPa
Poison's Ratio, ν	0.30
CTE, α	25.5 x 10^{-6} /^{o}C

3.2.7 Silicon Die

Ideally, the entire die is comprised of single silicon crystal without any grain boundaries. Silicon has fairly consistent properties through the temperature range of -55^{0}C to 125^{0}C, and as a result, isotropic material properties were used. It's properties are tabulated in Table 3.9.

Table 3.9 Material properties for silicon Die (CINDAS database, 1995)

Material Property	**Value**
Elastic Modulus, E	130.0 GPa
Poison's Ratio, ν	0.3
CTE, α	2.61 x 10^{-6} /^{o}C

3.3 Thermal loads

The thermal loading is based on the JEDEC 104B. The standard requires temperature cycling between –55 ^{o}C and 125 ^{o}C every twenty minutes , keeping the dwell time as 5 min at the two temperature extremes. The structure is assumed to be stress free at the melting temperature of Pb-free solder of 217 °C. It is allowed to cool down to room temperature (25 °C), and then the thermal cycling starts with ramp rate of 18 °C /minute. Figure 3.5 shows the time-temperature profile. Note upto five cycles are applied.

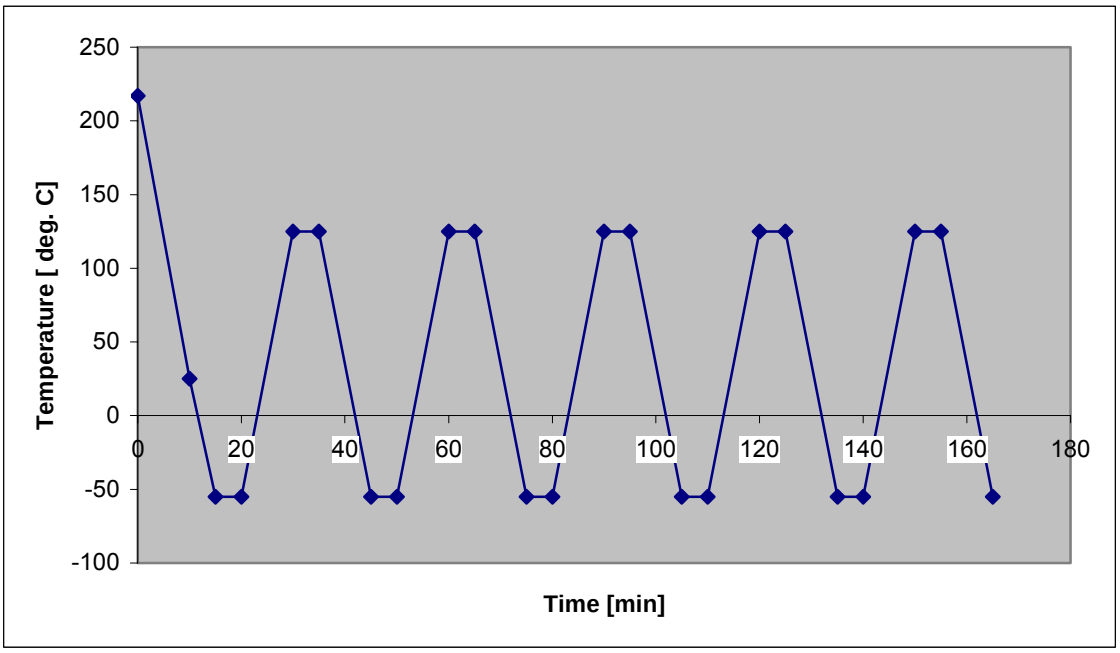


Figure 3.7 Thermal cycling profile applied on the FEM model.

3.4 Summary

A Global/Local FEA model was developed to capture the entire dimensional range from die length to intermetallic lengths. The FEA model incorporated non-linear material properties including elastic plastic properties for the new Pb-free solder. It also used Cu_6Sn_5 intermetallic properties. The results were obtained at the end of five thermal cycles when the stresses seem to stabilize. The results are compiled in chapter 4.

CHAPTER 4

FEM MODELING: RESULTS AND FAILURE ANALYSIS

The analytical results from the FEM model for different UBM thicknesses are presented in this chapter and the implications are discussed. The chapter begins with identifying the critical regions in the FCOB. It then discusses the potential failure mechanisms in the assembly, namely delamination of the critical interfaces. Finally solder fatigue evaluation is done.

4.1 Identifying critical regions

The critical regions in the FCOB are identified by first evaluating the stresses in the global model. This region is modeled as the cell model. Next, the interfaces of the cell model are assessed in detail for potential failure sites.

4.1.1 Critical region in the die: Global model

Von-misses stresses in the solder joints are calculated for locating the most stressed solder joint. It is found that the solder joint, furthest from the neutral point is the most stressed. Solder bumps near the symmetry are least stressed. Figure 4.1 shows the stresses in the solder joint at the room temperature, soon after reflow.

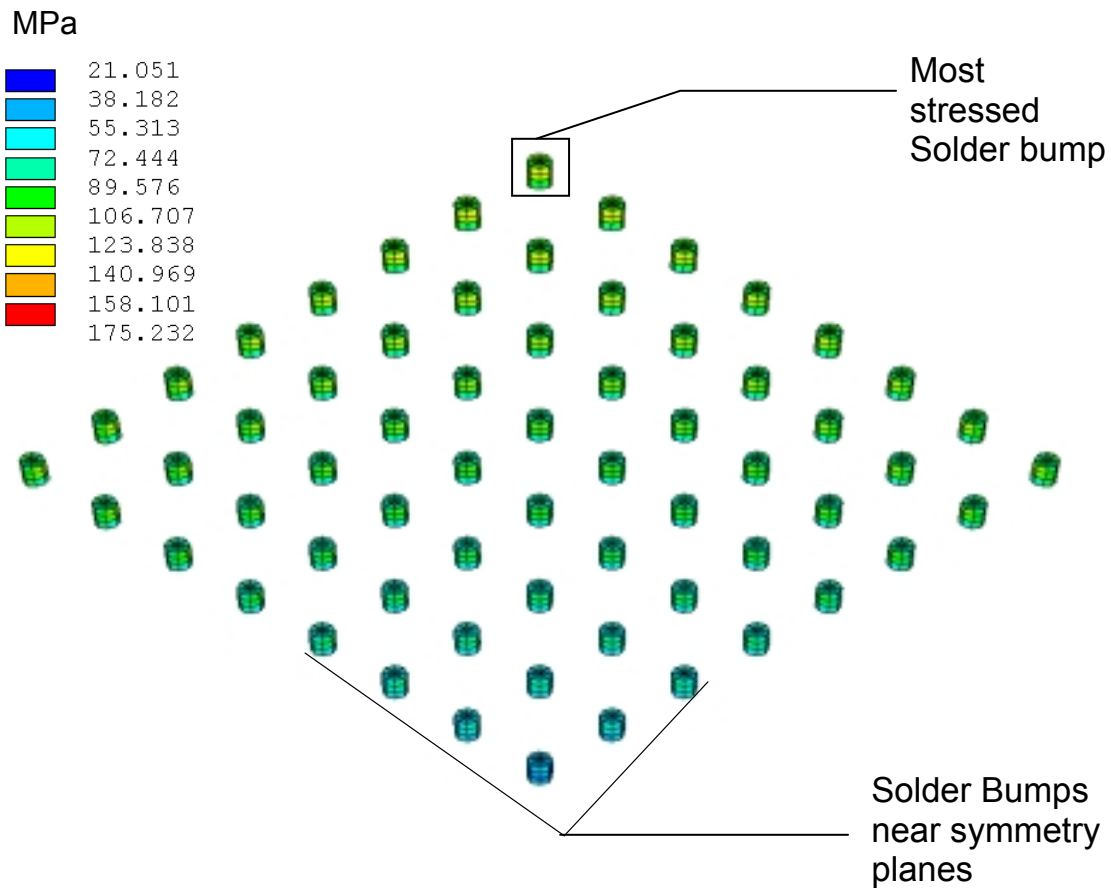


Figure 4.1 Von-misses stress in solder interconnects in the global model.

4.1.2 Critical interfaces: Cell model

Entire volume of the most stressed solder joint along with the FR4 and the silicon die and various UBM layers are modeled for the cell model. In order to identify the critical interfaces, a top down approach is taken. Figure 4.2 shows the cross section of the entire cell model, plotted for stresses. The critical regions are the UBM/IMC, Cu Pad/IMC and the corners of Cu pad and FR4. The stresses in the solder remain low due to the plastic flow.

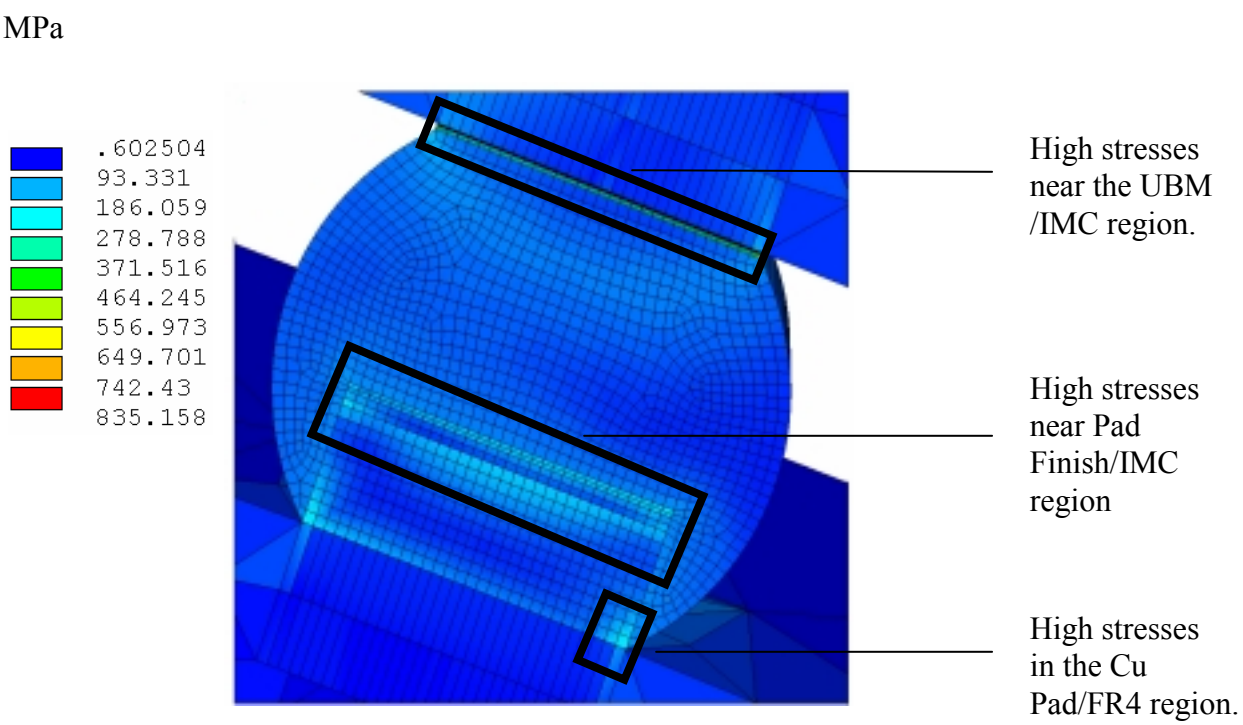


Figure 4.2 Cross section of cell model showing Von-misses stresses.

Having identified the critical interfaces we plot these individually in order to locate the individual metal/alloy layers. Figure 4.3 shows the various UBM layers and the IMC formed after reflow. Nickel is highly stressed and at the corners of the IMC. Therefore, the Ni-IMC layer could potentially delaminate.

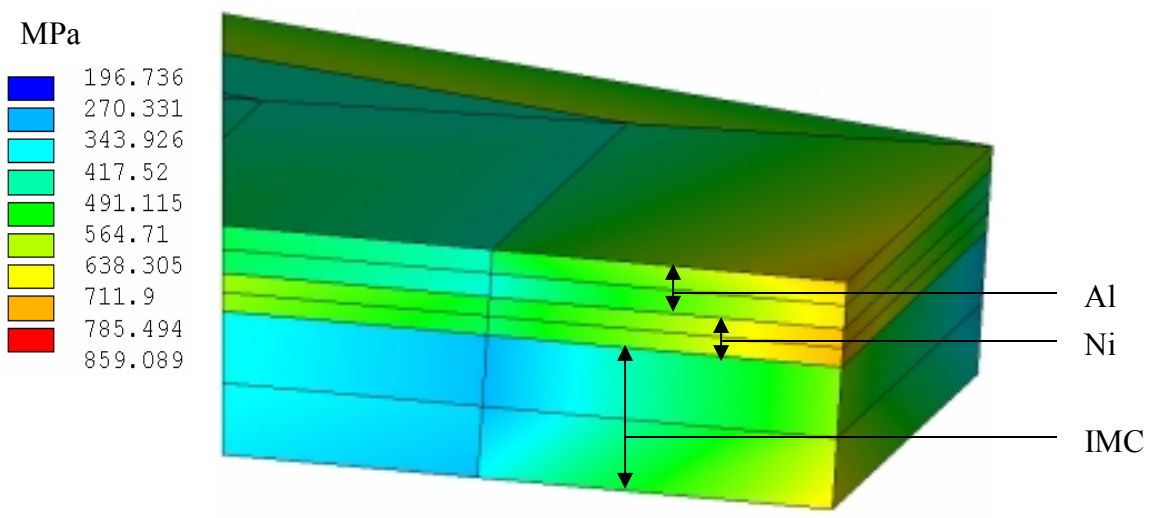


Figure 4.3 Stresses in UBM/IMC layers.

Figure 4.4 shows the Pad finish/IMC region. The IMC layer is highly stressed, along with the Cu pad/Ni interface regions.

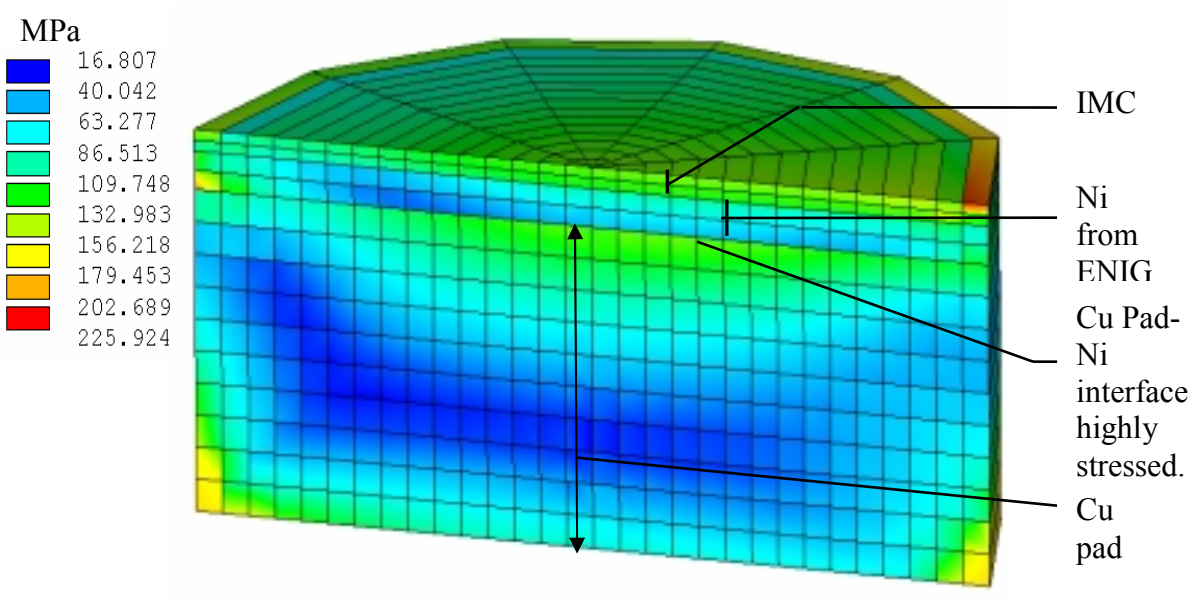


Figure 4.4 Stresses in pad finish/IMC region.

Thus the critical interfaces identified are:

a. On the UBM side:

1. Ni-IMC

and on the Pad side:

1. IMC-solder interface

2. Cu pad-Ni interface.

These highly stresses interfaces can delaminate and induce cracks.

4.2 Failure evaluation

4.2.1 UBM-IMC: delamination

Delamination of the Ni-IMC layer can occur, because of high interfacial stresses. Delamination is caused by high peel (σ_{yy}) and shear stresses (τ_{xy} ,τ_{yz}). These stresses would depend on the IMC layer thickness formed after reflow. This IMC layer formed immediately after reflow has the same thickness as that of the Cu layer present in the assembled Flip-chip. Figure 4.5 indicates that the maximum peel stress experienced at the the Ni-UBM interface is at -55 ºC. And this maximum peel stress is almost the same for different thicknesses. But at 125 ºC, the thickest UBM layer of 1.2 μm shows higher stress. On evaluating the shear stresses (τ_{xy} ,τ_{yz}) in Figure 4.5 and 4.6, we see that the thicker IMC layer (1.2 μm)shows least stress. In general is safe to conclude that peel stress variation is not much with IMC thickness. But the shear stresses for the 1.2 micron are considerably less.

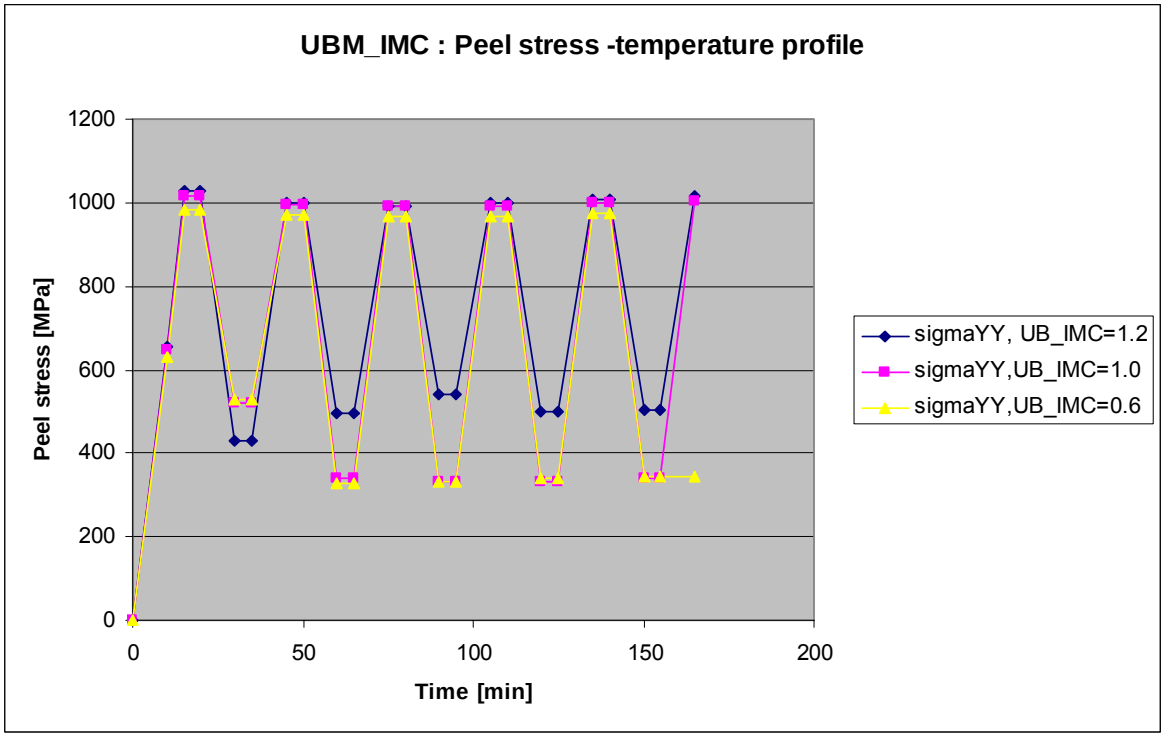


Figure 4.5 UBM(Ni)-IMC interface: peel stress (σ_{yy}).

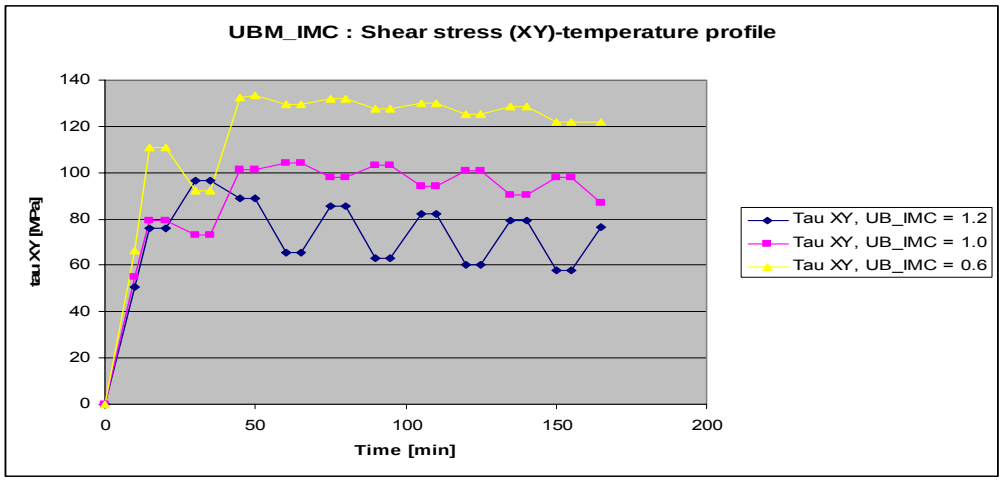


Figure 4.6 UBM(Ni)-IMC interface: shear stress τ (xy).

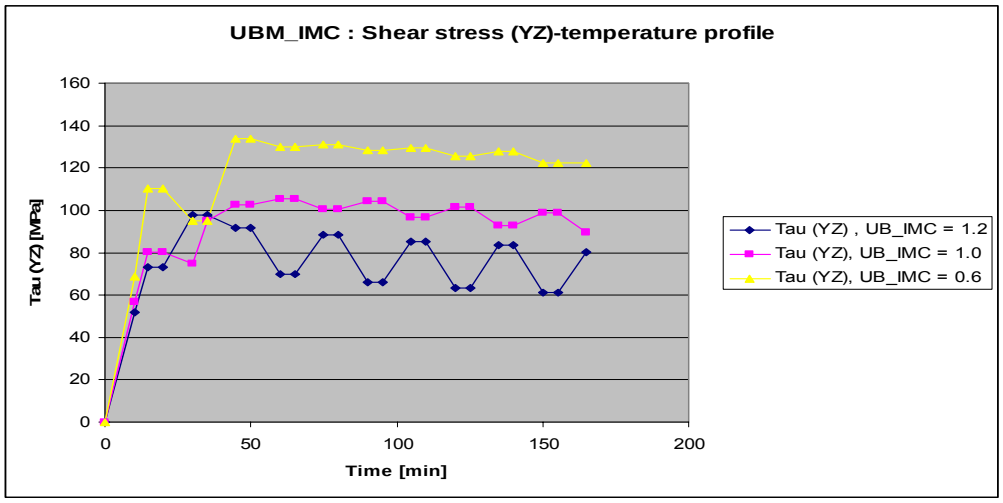


Figure 4.7 UBM(Ni)-IMC interface: shear stress τ (yz)

Table 4.1: UBM(Ni)-IMC : maximum interfacial stresses

IMC thickness	**Maximum peeling stress (σyy) MPA**	**Maximum shear stress (τxy)**	**Maximum shear stress (τyz)**
0.6	974.319	128.459	127.813
1.0	997.585	90.291	92.813
1.2	1007	79.513	83.294

4.2.2 Cu Pad-Ni (ENIG)): delamination

Delamination of the Cu Pad-Ni layer can occur. Again, this is because of high interfacial stresses. The fracture can propagate due to the brittle nature of the phosphorous during Nickel electroless-plating. The high interfacial stresses show that the delamination can initiate easily and then propagate causing fracture. Figure 4.8, 4.9, 4.10

indicates that the UBM thickness does not affect the stresses on the pad side. But as expected, lower the temperature higher is the stress.

Table 4.2: Cu pad-Ni (ENIG pad finish): maximum interfacial stresses

IMC thickness	**Maximum peeling stress (σyy) MPA**	**Maximum shear stress (τxy)**	**Maximum shear stress (τyz)**
0.6	199.987	199.896	197.582
1.0	95.582	97.239	97.253
1.2	95.543	95.538	94.993

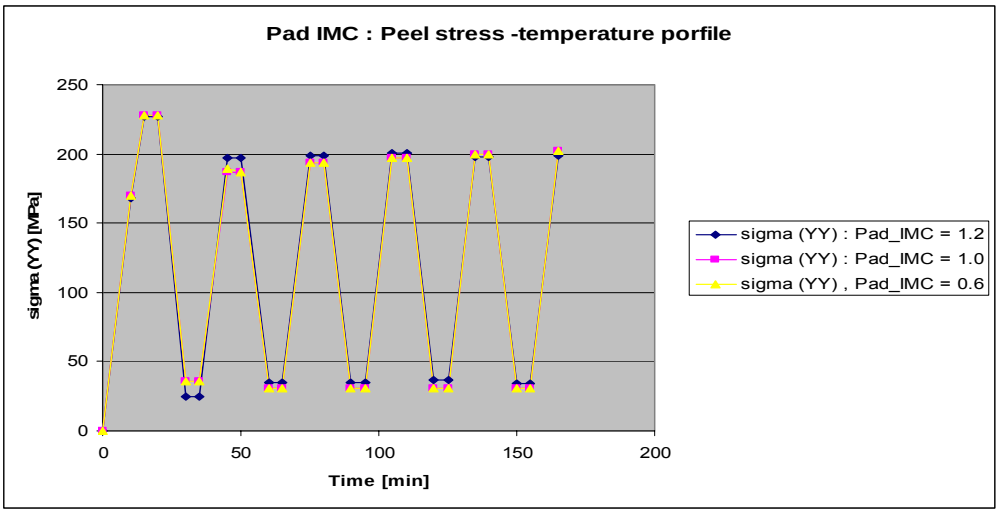


Figure 4.8 Cu pad-Ni (ENIG pad finish) interface: 9eel stress (σ_{yy}) .

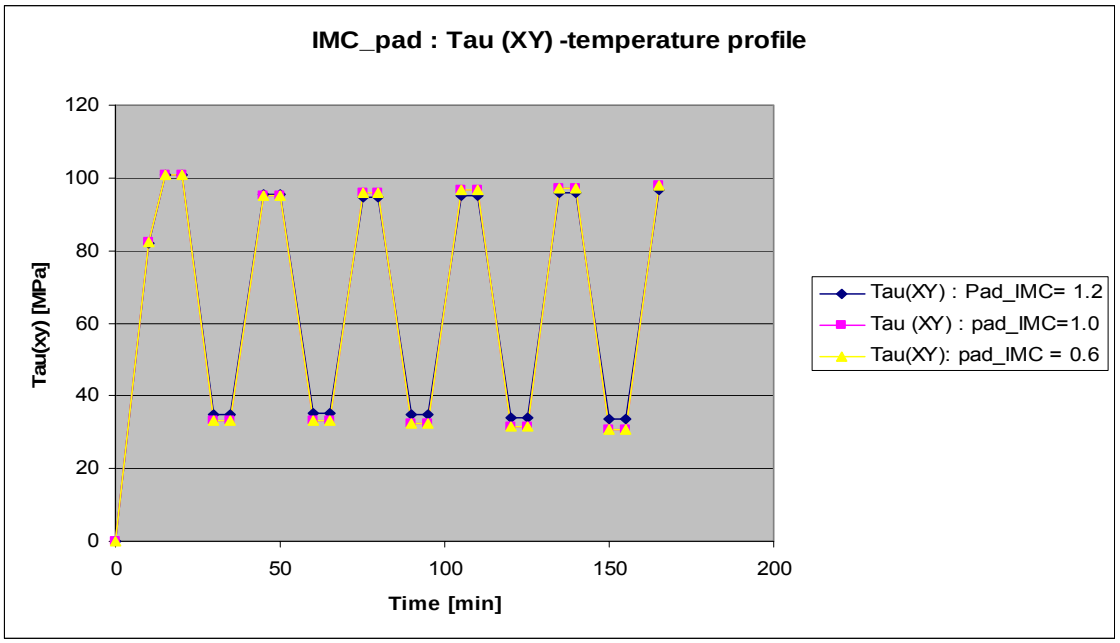


Figure 4.9 Cu pad-Ni (ENIG pad finish) interface: shear Stress (τ_{xy}).

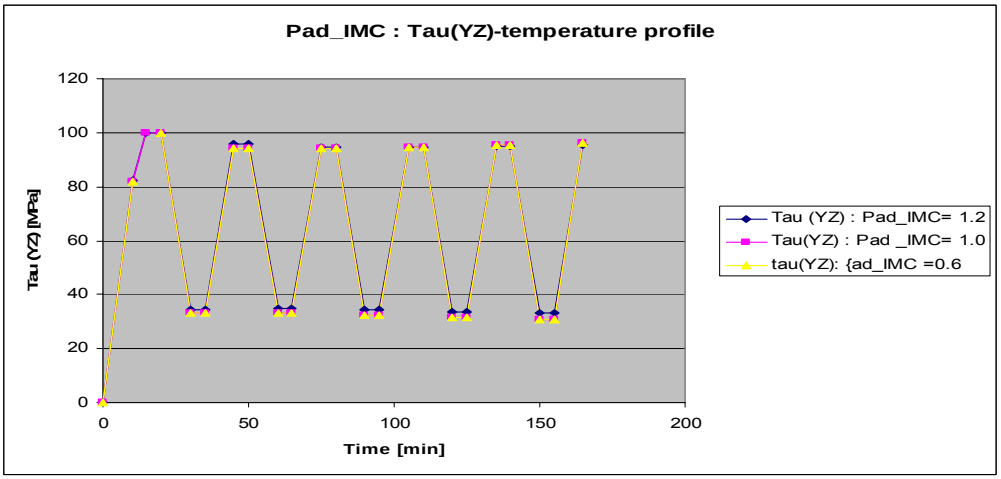


Figure 4.10 Cu pad-Ni (ENIG pad finish) interface: shear Stress (τ_{yz}).

4.2.3 Solder joint fatigue

In general, fatigue damage is evaluated depending on the number of cycles that a material or component is expected to undergo before it fails. The fatigue failure is expected to initiate at areas of stress concentrations due to cyclic loading. As the package is cyclically loaded in tension and compression (due to high and low temperatures), yielding may occur. When the stress is large enough to overcome the yield stress of the material, plastic deformation occurs in its cyclic loading. To predict low cycle fatigue for ductile metal and solder, the Coffin-Manson's equations that are experimental fits are often employed.

The damage metric considered in this study is equivalent plastic strain range. Greater the plastic range, less the number of cycles to failure and therefore decreased reliability. The equivalent plastic range can be computed from the plastic strains at two different temperature points from the load history. Section 2.3.2 details the method of computing equivalent plastic range from six individual strain components. The equivalent plastic range is calculated for each element of the solder paste in an entire temperature cycle. Figure 4.11 shows that strain rate stabilizes after 5 thermal cycles. Note that the IMC thickness of 1.2 micron reduces the strain considerably. This is because of the less concentration of stresses in the top region of the solder which is most critical. Appropriate constants for the Coffin-Manson equations for the new Pb-free solder can then be used to predict the fatigue life.

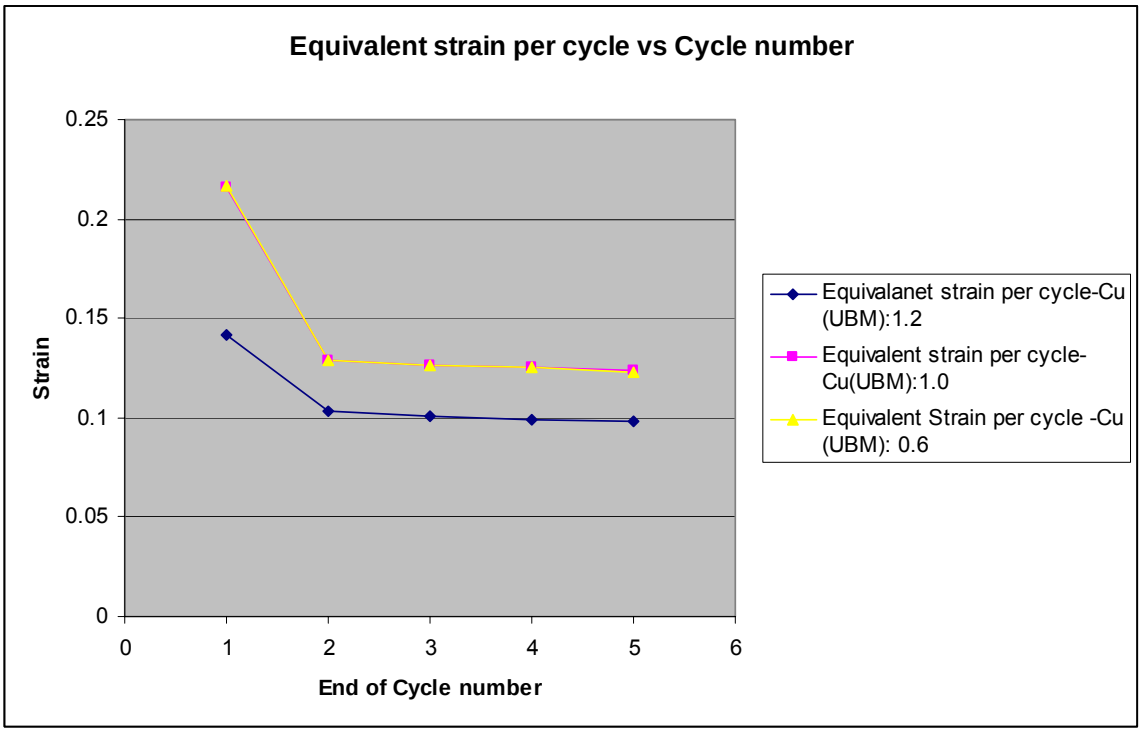


Figure 4.11 Solder joint – equivalent strain per cycle.

4.3 Summary

FEA modeling carried out to predict the stresses at various the interfaces in the flip-chip on board package during thermo-mechanical loading. The critical interfaces identified are are intermetallic/UBM system, and substrate pad/solder interfaces. The time and temperature dependent deformation accumulates with repeated cycling and ultimately causes delamination, solder joint cracking and interconnect failure. Effects of IMC thickness on the delamination have been discussed. Equivalent plastic strange is computed for solder joint fatigue prediction.

CHAPTER 5

EXPERIMENTS AND DISCUSSION

The experimental work carried out as part of this research is discussed and the results are presented in this chapter. This chapter begins with an overview of the various parameters in FCOB assembly. These are divided into three separate experiments. First experiment compares the thermo-mechanical reliability of the eutectic Pb-based solder and Pb-free solder. It relates the IMC formation across these solders to the reliability results. Next section discusses the Experiment 2, where the effect of UBM thickness on IMC formation is evaluated along with the reliability results. The final experiment looks into the assembly with various substrate pad finishes. It compares them for the IMC formation and assembly conditions.

5.1 Experiments and Parameters

FCOB assembly involves a slew of parameters. Modeling results in Chapter 4 identified the intermetallic/UBM system and substrate pad/solder interfaces as the most critical in terms of stresses. Hence the three important parameters identified are the, i. solder, ii. UBM and iii. substrate pad finish. These also affect the IMC formation and growth. Hence experiments are designed in order to understand role of these parameters in the FCOB reliability. Table 5.1 shows the various parameters evaluated. Experiment 1 primarily compares intermetallic formation in eutectic solder vis-à-vis Pb-free solder and its affect on reliability. Experiment 2 compares the affects of changing UBM thickness on the IMC formation and growth. Experiment 3 aims at evaluating

different substrate pad finishes. Experiment 2 and 3 are carried out only with Pb-free solder.

Table: 5.1 Parameters studied in thermo-mechanical reliability experiments

Experiment	**Parameter**	**Parameter Values**
Exp 1	Solder	Eutectic solder (63Sn-37Pb)
		Pb-free solder (Sn95.5-Ag3.8-Cu)
Exp 2	UBM (Al/Ni/Cu)	Cu = 1.2 μm
		Cu = 1.0 μm
		Cu = 0.6 μm
Exp 3	Substrate pad finish/Top surface metallurgy	Direct immersion silver
		Organic solderability preservative (OSP)
		Direct immersion gold

5.2 Materials

This section details the various materials used in the experiments. The flip-chip components were purchased from Delphi-Electronics in a waffle pack. These FA-10s are non-functional silicon test dies and have a daisy chain pattern incorporated into the I/O redistribution wiring layer. The daisy chain pattern is useful because only two points need be tested for continuity on the substrate, provided the printed wiring board is designed correctly with a matching daisy chain pattern. Each flip-chip is 1 cm x 1cm with 1268

I/O's. All the the flip-chip have UBM metallization layers as Al (4000 A^0), Ni/7%V (3250 A^0), and Cu (6K A^0, 8K A^0, 10K A^0, 12K A^0). The flip-chips are either Pb-free bumped (Sn95.5-Ag3.8-Cu) or eutectic Pb bumped. The flux used is Alpha 615-15 RMA type and the Capillary flow underfill for the assembly is Loctite Hysol FP4526. An unassembled flip-chip is shown in Figure 5.1.

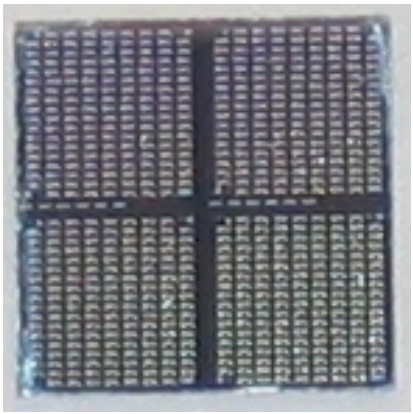


Figure 5.1 Flip-Chip.

The Gerber files for the PWBs are shown below in Figure 5.2. 5.2(a) shows the overall layout of the substrate, and 5.2(b) shows close up view of one of the board sites for placement. The boards were manufactured by Tech Circuits. The boards themselves were 625 µm thick. The FR4 has a glass transition temperature of 170 °C. The base conductors is ½ oz. Cu. Table 5.2 lists the material specifications.

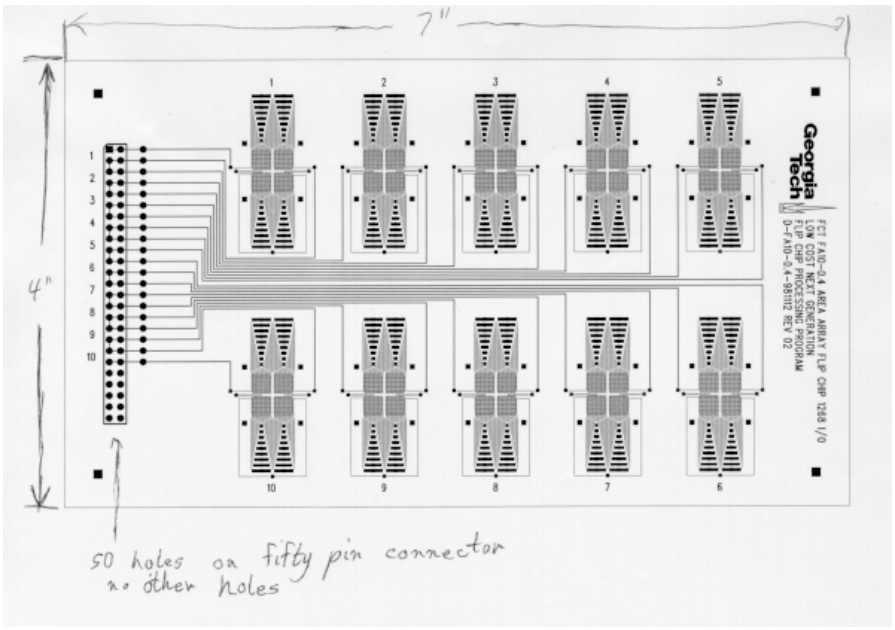


Figure 5.2 FR4 Board. (a) Test substrate (b) Close-up of test site

Table 5.2: Material specifications

Material	**Specifications**
Daisy chained flip-chip	1 cm x 1 cm pitch : 250 um solder height 125 um 1268 solder bumps (95.5Sn-3.8Ag-Cu, 63Sn/37Pb) UBM : Al (4000 A^0), Ni/7%V (3250 A^0), Cu (8000 A^0)
FR4	Pad finish is ENIG Ni(4.5 µm), Au (0.1-0.2µm)
Underfill	Capillary Flow Underfill (Loctite Hysol FP4526)
Flux	Alpha 615-15 RMA

5.3 Methods

The PRC assembly facility was used to assemble the FA-10 packages on the PWB and prepare them for thermal cycling and aging in the chambers. The general assembly process is outlined below.

5.3.1 Assembly

Step 1: Placement and Reflow

The individual placement sites are cut off from the board bye a saw. The chip placement system used has an offset, hence care must be taken during placement to obtain proper alignment.

Step 2: Alignment check

After the chips have been placed, an alignment check is performed in the *Fein Focus X-Ray chamber* used, which is shown in Figure 5.3.

Figure 5.3: X-Ray machine.

Step 3: Reflow

After X-ray inspection, the packages are reflowed in the *Electrovert Omni Flo 5* shown in Figure 5.4. It is a five region convection reflow oven with a sixth cool down region, and has heaters on the top and bottom which can be programmed for many different reflow profiles. The speed of the package through the oven can also be changed, and for standard eutectic, the speed was 20 in/s. The reflow profile is dependent on several factors, some being solder content, package size and board thickness. The oven temperatures and the reflow profiles used for eutectic solder and Pb-free solders are shown in Tables 5.3, 5.4 and Figures 5.5, 5.6.

Figure 5.4 Reflow Oven.

Table 5.3 Reflow temperatures in oven for Sn/Pb eutectic

	Region 1	**Region 2**	**Region 3**	**Region 4**	**Region 5**	**Cool down**
Top	100 °C	150 °C	150 °C	180 °C	230 °C	180 °C
Bottom	100 °C	150 °C	150 °C	180 °C	230 °C	180 °C

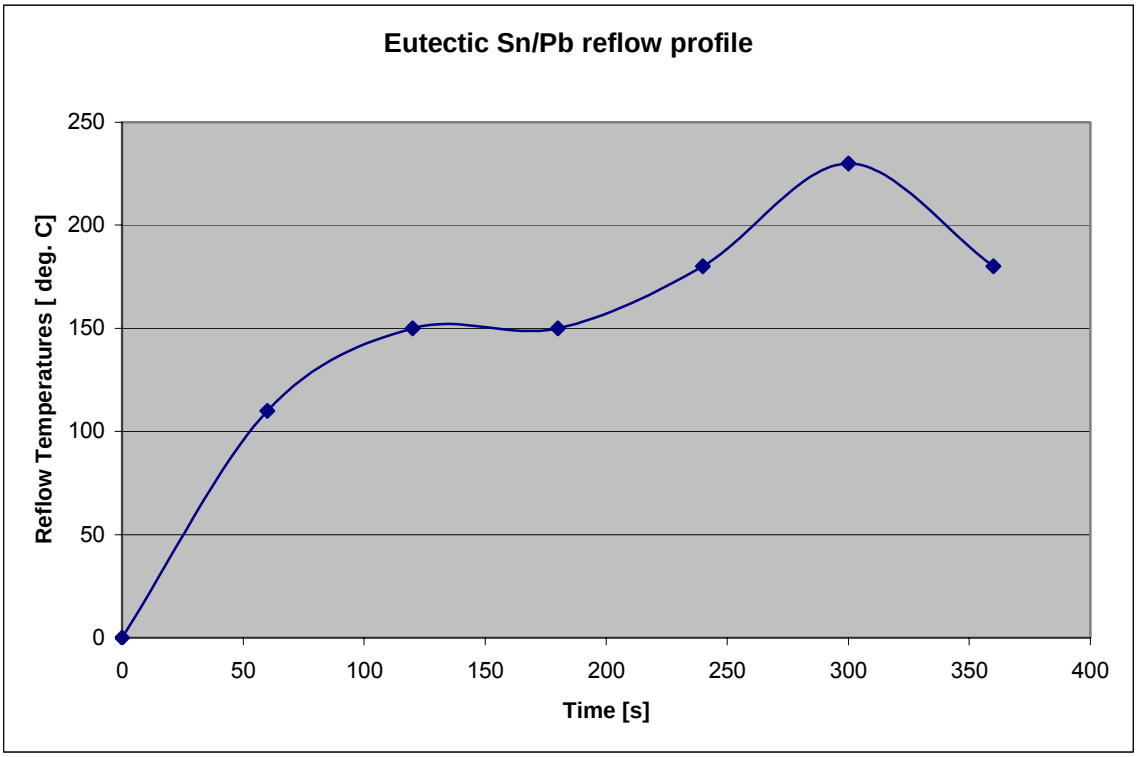


Figure 5.5 Reflow profile for eutectic Pb/Sn solder.

Table 5.4: Reflow temperatures in oven for Sn-Ag-Cu solder

	Region 1	**Region 2**	**Region 3**	**Region 4**	**Region 5**	**Cool down**
Top	170 °C	180 °C	210 °C	250 °C	270 °C	103 °C
Bottom	170 °C	180 °C	210 °C	250 °C	270 °C	103 °C

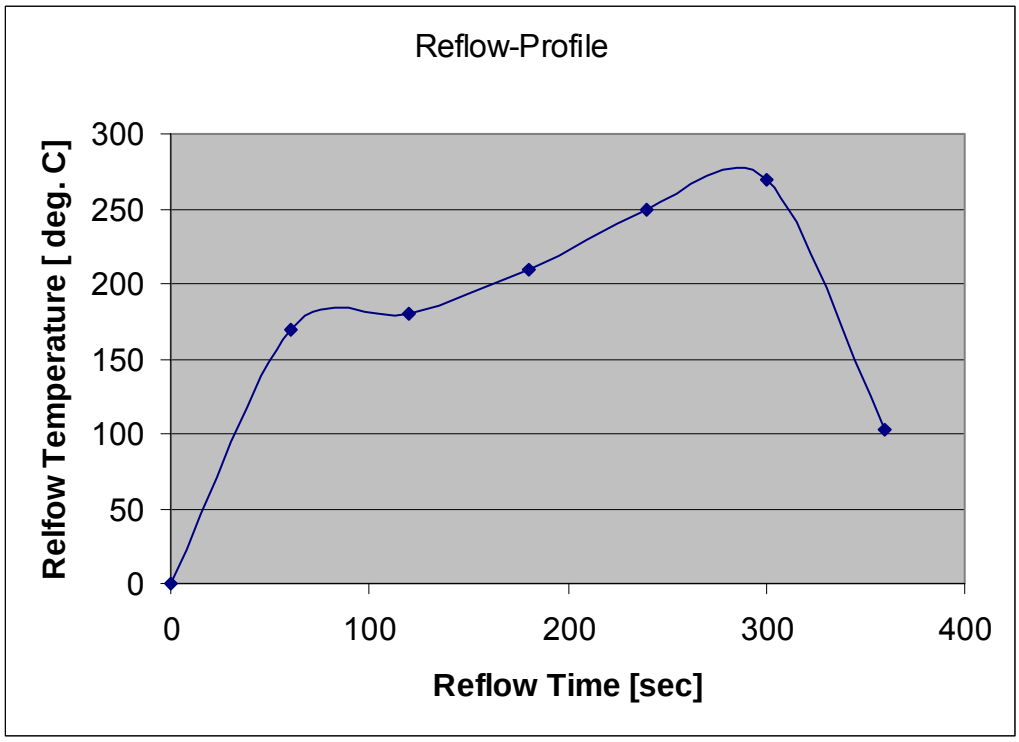


Figure 5.6 Reflow Profile for Sn3.8-Ag0.7-Cu solder.

Step 4: Underfill dispensing

Loctite capillary reflow underfill was dispensed at 45 psi for 15 seconds ensuring 17-19 mg dispensed. It was then heated for 60 sec on 100 ^{0}C hot plate to decrease its viscosity, and then cured at 165 ^{0}C for 15 minutes. The thermo-mechanical tests used to simulate the actual field conditions are described below.

5.3.2 Testing

1. Thermal Aging

The assembled chips are subjected to thermal aging at 100, 200, 350,500 hrs at 150 ^{0}C as per JESD22-A103-B. This ensures the intermetallic growth. Figure 5.7 shows the thermal aging chamber.

Figure 5.7 Thermal aging chamber.

2. Thermal Cycling

To experimentally test these components, thermal cycling chambers that are able to change the temperature of the components based on the thermal profiles outlines in Section 3.3 are required. However, at Georgia Tech, only two air-air thermal shock chambers and one air thermal cycling chamber were available, Unfortunately, the thermal cycling chamber did not have the capacity to reach -55 ºC, so the thermal shock chambers were required. The difference between the chambers is that usually a thermal cycling chamber has only one chamber, and the ambient temperature within the chamber is changed according to the profile developed. A thermal shock chamber, such as the chamber in Figure 5.8, uses two different zones, each at different temperatures, and carries the parts from one chamber to the next directly, through an internal staging mechanism that travels from one chamber to another.

Figure 5.8 ESPEC liquid to liquid thermal shock chamber.

In this specific chamber, the hot chamber is the top chamber, and the bottom chamber is the cold chamber. The problem with the thermal shock chamber is that it cannot control the ramping rate of the package.

The reliability was evaluated with liquid-liquid thermal shock tests. Test vehicles were subjected to a thermal shock between –55^{o}C to 125^{o}C using liquid media. Figure 5.9 shows an approximate schematic of the thermal cycle used for these tests.

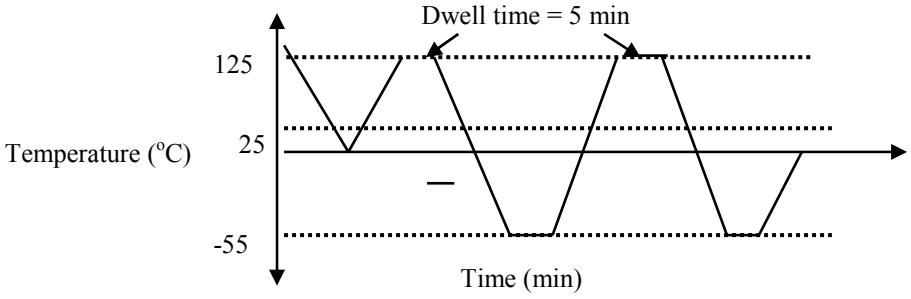


Figure 5.9: Schematic of thermal cycle for reliability tests.

3. Electrical continuity Measurement

The assembled chips were evaluated for electrical resistance after reflow and after set hours of aging and thermal cycles. The resistance increases to a very high value in case of an electrical open ; that may arise due to solder joint failure or delamination of the interfaces. The measurements were carried out using *Keithly 200 Multimeter*.

4. Bump Shear and die shear test

Solder bump shear test is performed on the aged Sn-Ag-Cu and Sn-Pb dies to evaluate the UBM performance. The instrument used was Dage Shear 4000 Tester. Die shear on assembled and aged flip-chips is carried out with a tool lift off height 15 µm and shear speed of 50 µm/s. The corresponding values for bump shear carried out on non assembled flip-chips are 15µm and 5 µm/s respectively. The sheared surfaces are examined using optical and electron microscopy.

Figure 5.10: Dage series 4000-PA.

5. Microstructure observation

In order to study the interfacial reactions, after heat treatment, the samples are mounted in epoxy resin and ground using Silicon Carbide (SiC) and finally polished upto 0.5µm in alumina suspensions. The polished sample is then etched in 10% HNO_3 solution for upto 10 seconds depending on the solder amount to be etched away .The interfacial microstructure observation is performed using the two scanning electron microscopes (SEMs) shown in Figure 5.11 and Figure 5.12.

Figure 5.11: LEO 1530 Thermally-Assisted FEG Scanning Electron Microscope (SEM).

Figure 5.12: Hitachi S800 FEG scanning electron microscope (SEM).

5.4 Thermo-mechanical reliability of Pb vs Pb-free: Experiment 1

This experiment aims to evaluate the thermo-mechanical reliability of Pb–free solder (Sn95.5-Ag3.8-Cu) in comparison to conventional eutectic (Sn63-Pb37) solder. Figure 5.13 shows the experimental design to isolate the effects of (1) thermal aging (at 150 ºC) and thermal cycling (-55 °C to 125 °C) on Pb-free flip-chips (Sn95.5-Ag3.8-Cu0.7) with respect to standard eutectic (Sn63-Pb37) joints. Figure 5.13 shows the experimental design of only Pb-free solder. Similar design is used for the Pb-based solder. The pad finish used is ENIG in this experiment.

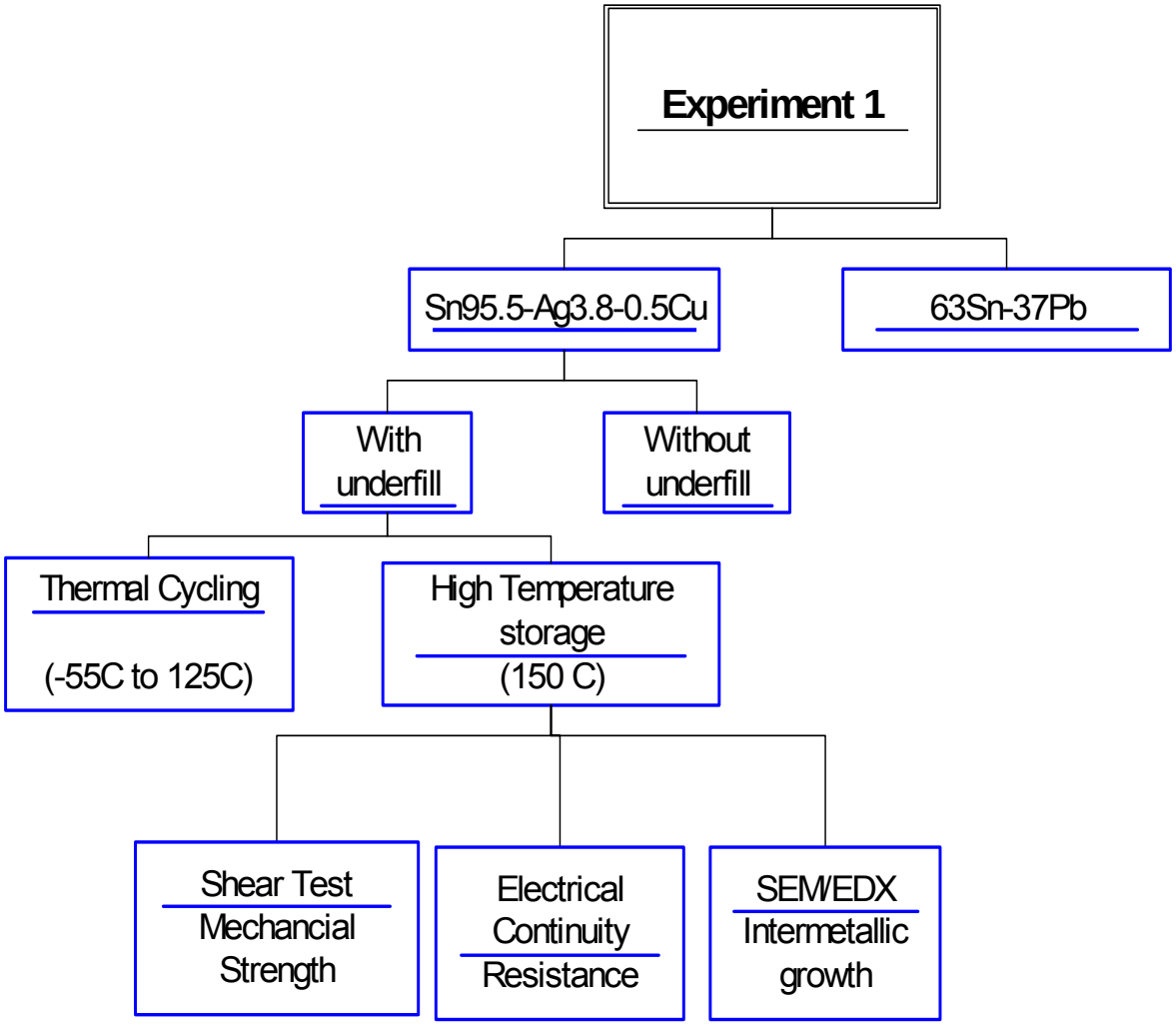


Figure 5.13: Design of Pb vs Pb-free: Exp1

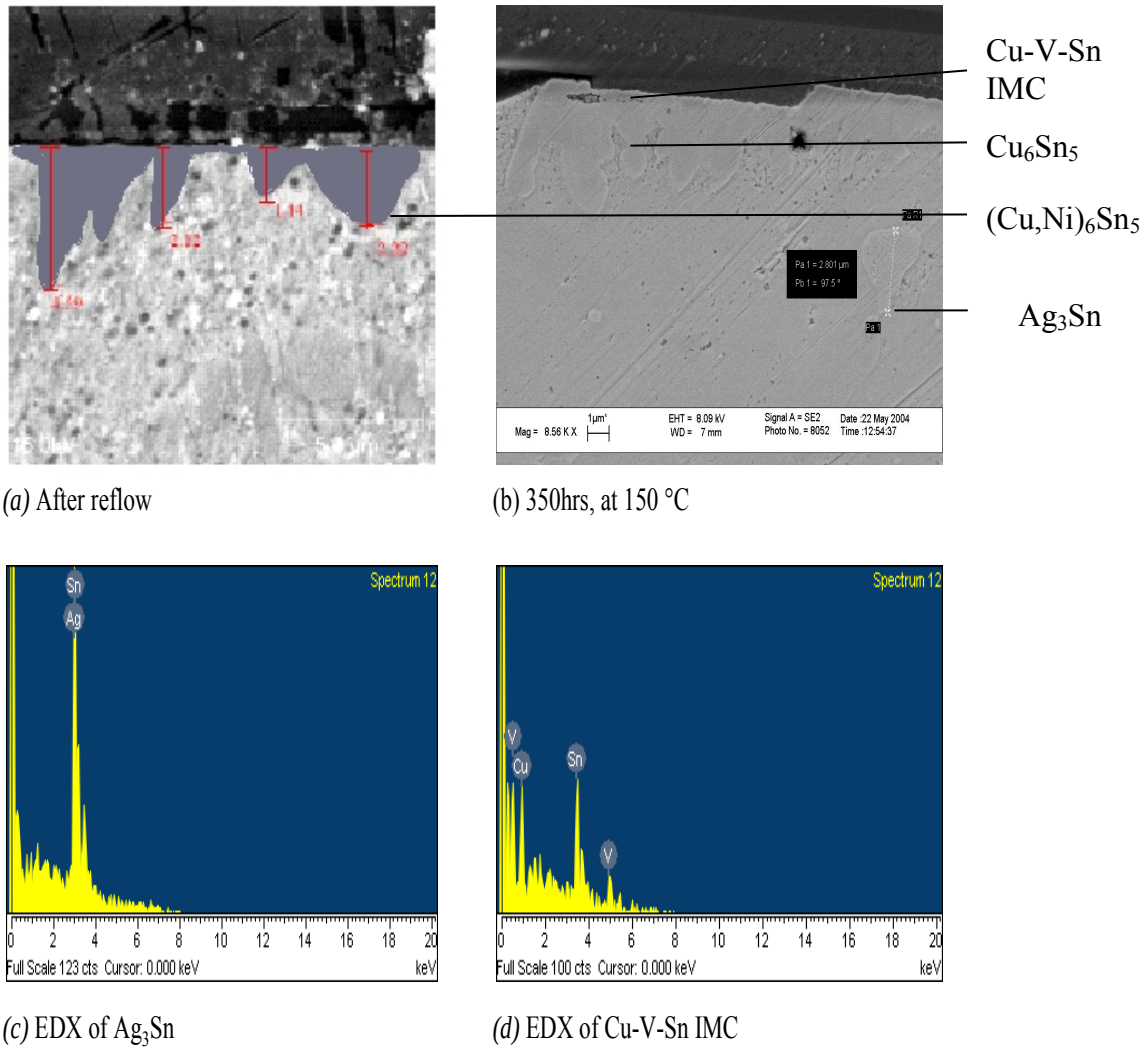
5.4.1 Intermetallic formation

IMC formation takes place on the UBM-solder interface when the wetting metallization layer (Cu) dissolves. Similarly on the substrate pad side, the Au of the ENIG diffuses into the matrix and and IMC is formed at the Ni--solder interface.

UBM-solder side:

After reflow the $(Cu,Ni)_6Sn_5$ IMC is formed as is seen in Figure 5.14 (a). This IMC grows with time; but as aging continues Ag_3Sn and (Cu-V-Sn) intermetallics are

also formed. Moreover Ni of the UBM diffuses hence only Cu_6Sn_5 remains. Figure 5.14(b). shows the Cu-V-Sn IMC at the interface, while Ag_3Sn is in the bulk of the solder. The EDX analysis of the microstructure confirms this. On the other hand for the Pb-Sn solder, a $(Cu,Ni)_6Sn_5$ IMC is formed. It similar to that formed in Sn-Ag-Cu solder, but the thickness is less. The thickness formed is 2.52 µm for Sn-Ag-Cu and for Sn-Pb solder it is 1.56 µm. Figure 5.15 shows the IMC formation in Sn-Pb interface.



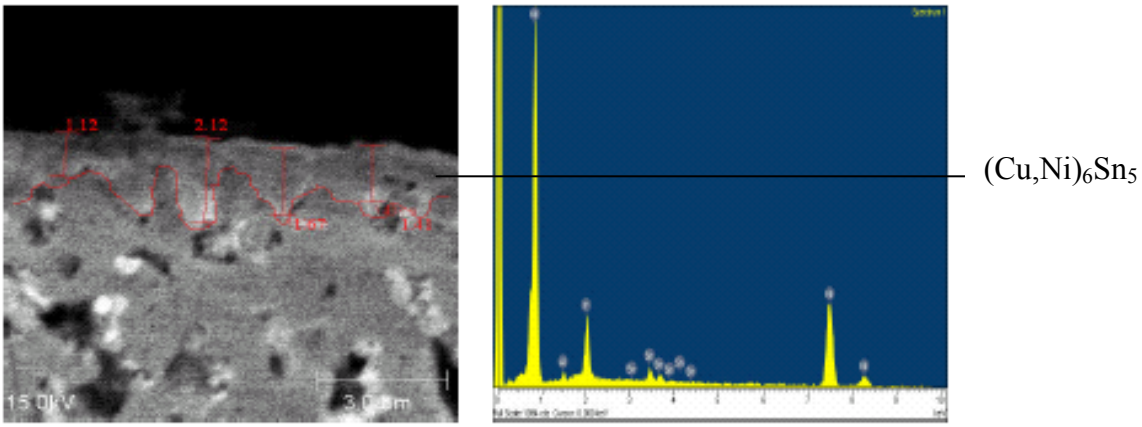
(a) After reflow

(b) 350hrs, at 150 °C

(c) EDX of Ag_3Sn

(d) EDX of Cu-V-Sn IMC

Figure 5.14 IMC on SnAgCu-UBM interface

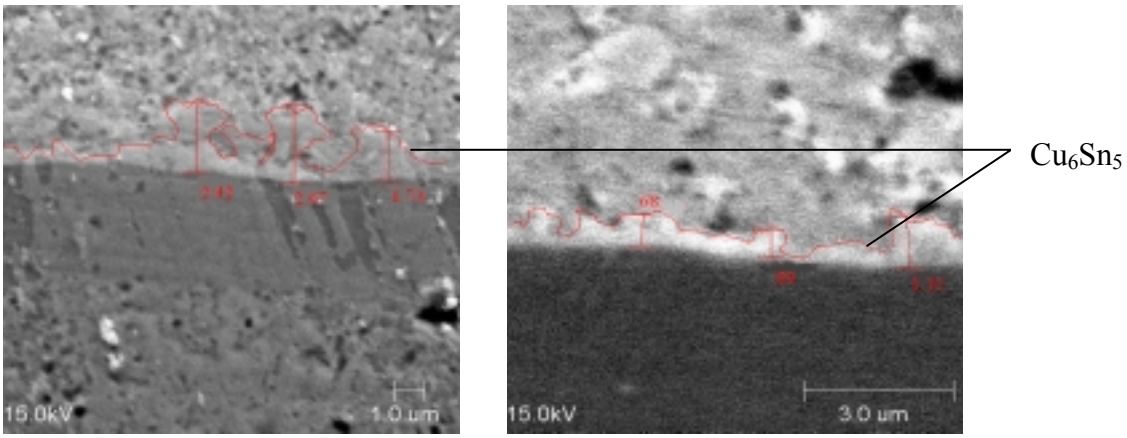


(a) (b)

Figure 5.15 IMC on Sn-Pb interface (a) after reflow (b) EDX of $(Cu,Ni)_6Sn_5$

IMC on Solder-pad interface

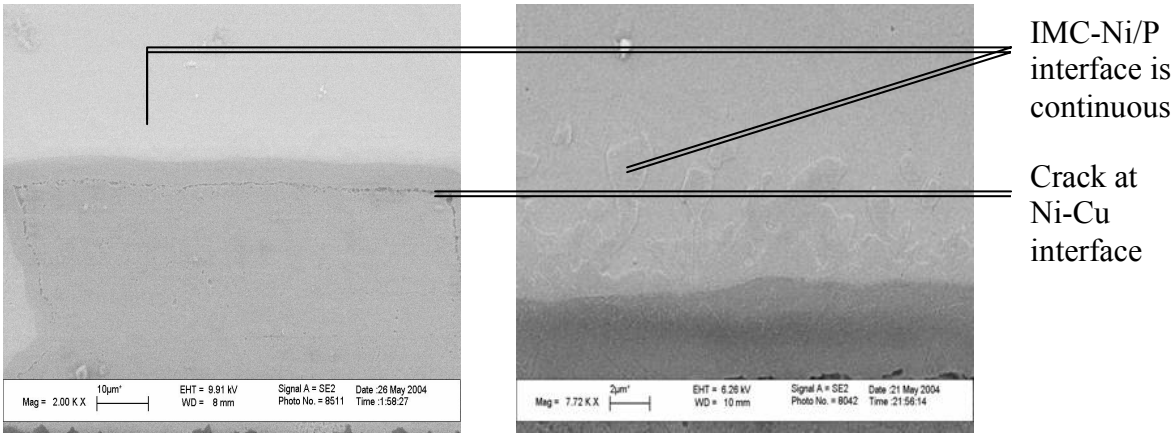
Cu_6Sn_5 IMC is formed having thickness of 2.27µm in Sn-Ag-Cu. This thickness result is used in the FEM modeling in Chapter 3 as well. A thinner layer of IMC of 0.92 µm micron is formed at Sn-Pb-ENIG interface. This is shown in Figure 5.16.



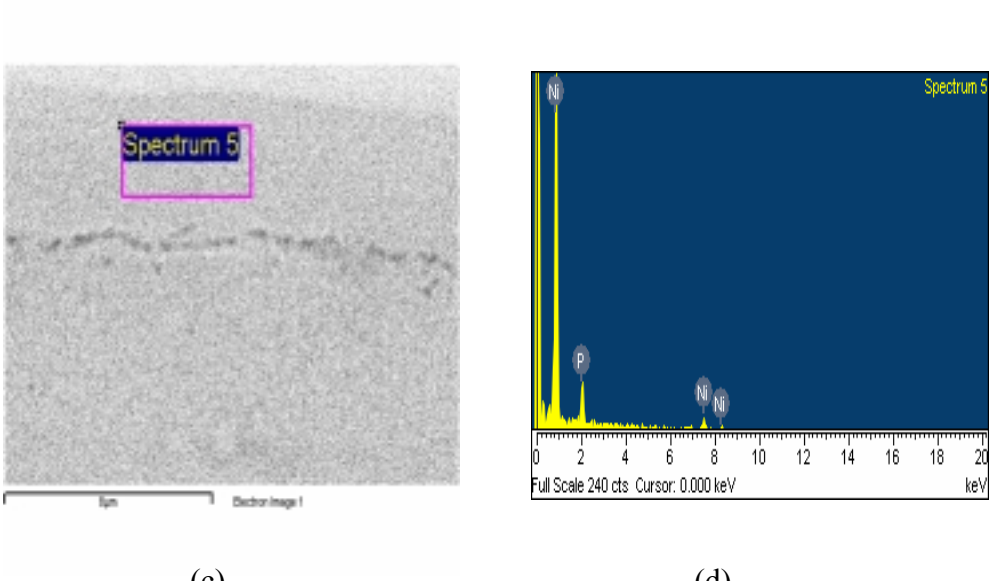
(a) *(b)*

Figure 5.16: IMC on Solder-Pad interface (a) SnAgCu as reflowed, (b) SnPb as reflowed

As the aging progresses the Cu pad-Ni (ENIG) layer starts to crack is seen in figure 5.17(a). The IMC-Ni/P(ENIG) layer remains intact, seen in Figure 5.17 (b). The EDX analyis of the region between the crack and the IMC, confirms that Ni-P brittle compounds are formed. These result in the cracking of the Cu pad-Ni interface. Figure 5.17 (c) shows the enlarged view of the region between crack and he IMC. EDX of the region is shown in figure 5.17(d).



(a) 350hrs at 150°C *(b) Enlarged view, 350 hrs at150°C*



(c) (d)

Figure 5.17 Crack seen at Cu pad-Ni/P(ENIG) interface in SnAgCu

5.4.2 Solder-UBM mechanical strength

Figure 5.18 plots the ball shear (BS) strength of the FA10 dies. The Sn-Ag-Cu ball joint shows rapid decrease in the strength after 100 hrs and then remains constant. SnPb shows almost same consistency across high temperature storage hours. Twelve bumps were sheared for each chip. The ball shear (BS) value of as reflowed (0 hrs HTS) Sn-Ag-Cu solder is two times higher then the corresponding value for Sn-Pb as seen in Figure 5.18. For Sn/Pb solder-UBM joint BS strength remains more or less constant throughout the HTS test. Statistically the SnAgCu – Ni/Cu UBM solder joint strength is more then the SnPb- Ni/Cu UBM across the HTS hours. Two Way Anova analysis is carried out. where the HTS hours are "blocked" and solder type is the "treatment". The results in Figure 5.19 confirm that the BS strengths are indeed different for the two solder types.

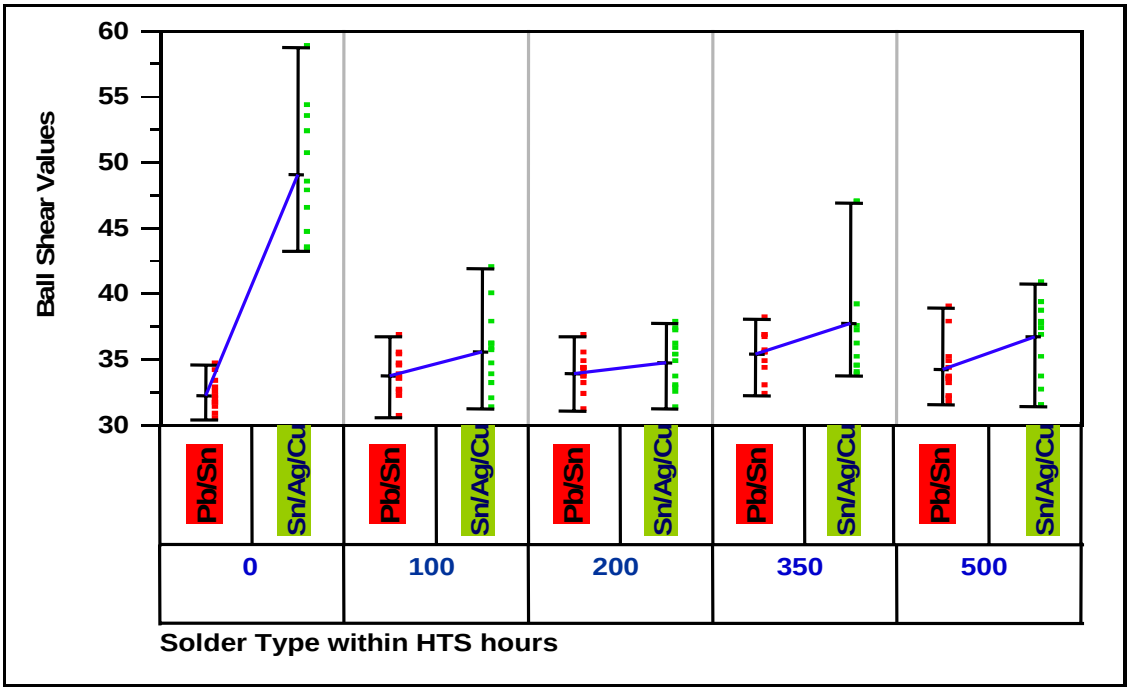
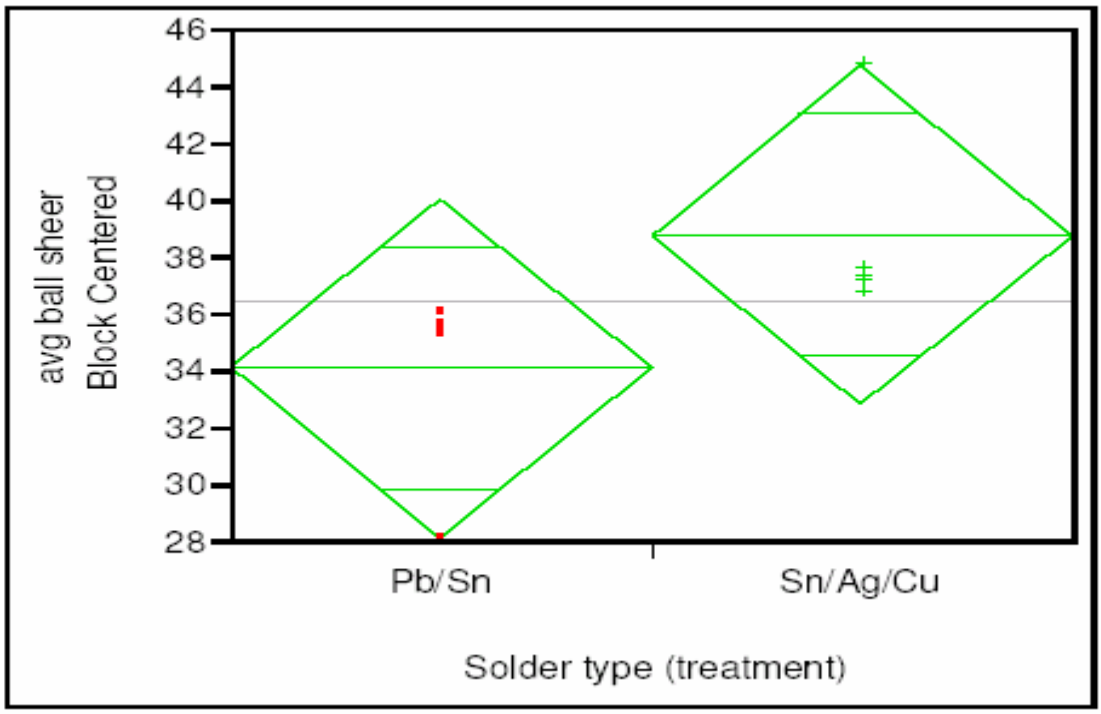


Figure 5.18 Ball shear values of Sn-Pb vs Sn-Ag-Cu across HTS hours



(a)

Source	*DF*	*Sum of Squares*	*Mean Square*	*F Ratio*	*Prob > F*
Solder Type(treatment)	1	32.807	32.807	7.659	0.050
HTS hours (Blokcing)	4	2.823	0.705	0.164	0.945
Error	4	17.133	4.283		
C. Total	9	52.764			

(b)

Figure 5.19 Two Way Anova of ball shear values of Sn-Ag-Cu and SnPb–UBM joints across HTS hours. (a) solder type against BS , (b) results table

5.4.3 Electrical continuity

(a) HTS results, Pb vs Pb- free

HTS test is carried out for upto 500 hrs and the failure rate is defined as the daisy chain resistance change of more then 20 percent. Application of underfill reduces the failure rate considerably for both SnAgCu and SnPb. Percentage change for both Sn-Ag-Cu and Sn-Pb daisy chains is observed to vary from 1 to 10 percent as shown in Figure 5.20 except for Sn-Ag-Cu, at 350 hrs. On analysis this anomalous behavior is identified due to high flux content during the assembly process for this flip-chip. Underfill increases joint life for SnPb as we see no failure even after 500 hours of Sn-Pb. This is seen in Figure 5.21. But for the Sn-Ag-Cu the increase is not much. This is because of needle shaped Ag_3Sn which is formed in the bulk of the solder as shown in Figure 5.14 (b).

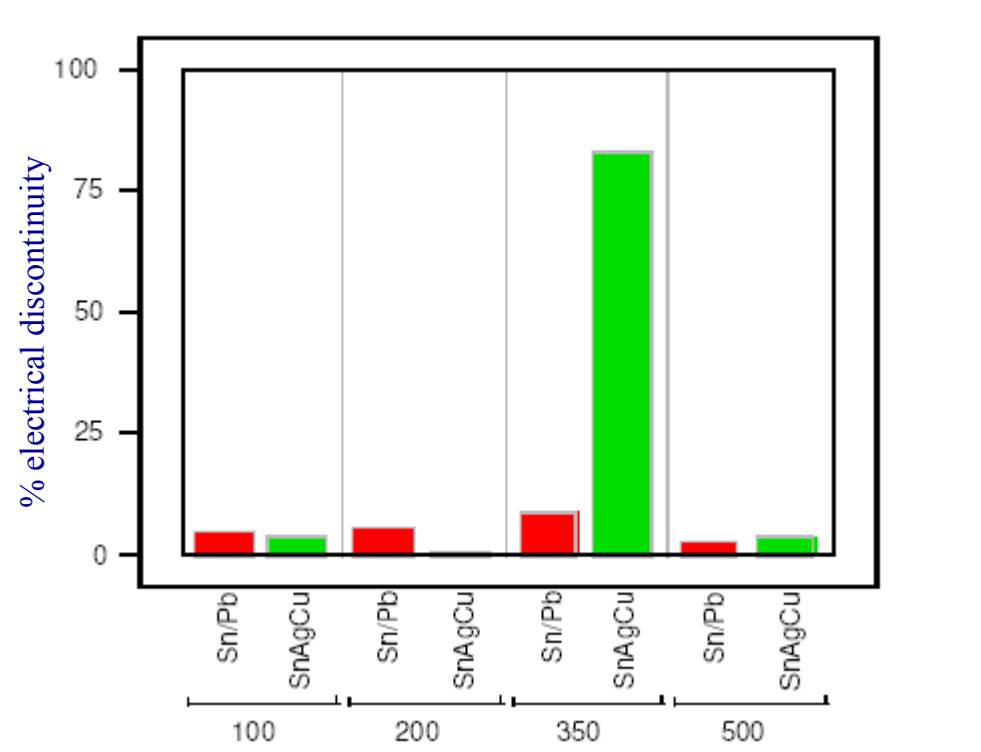


Figure 5.20. Electrical continuity without underfill (HTS)

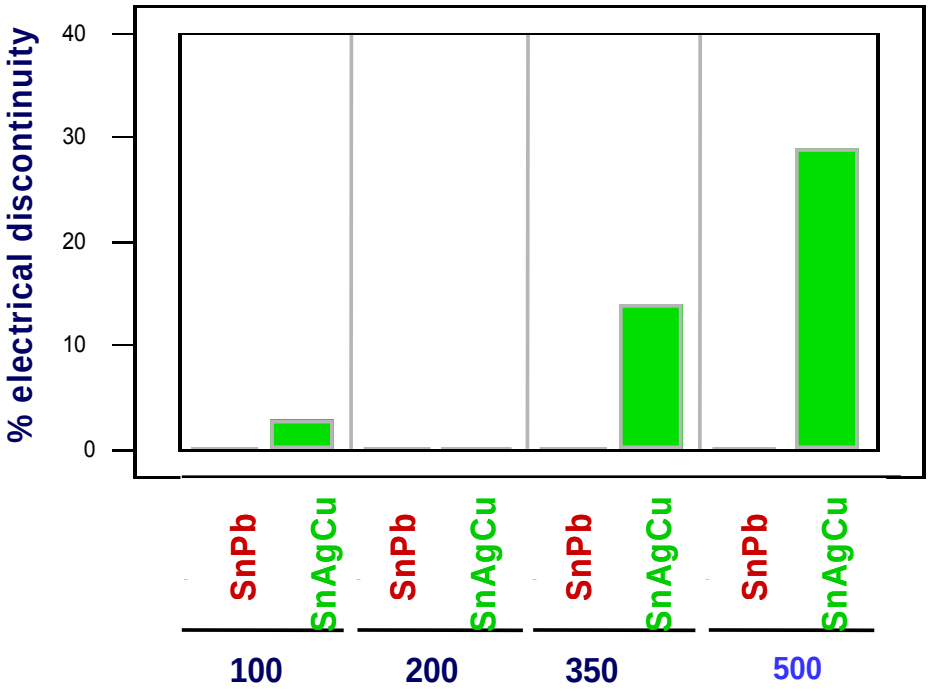


Figure 5.21 Electrical continuity with underfill (HTS)

(b) Thermal Shock results, Pb vs Pb- free

Thermal shock testing was done on the assembled chips. Without the use of underfill, both SnPb and SnAgCu completely fail (no daisy chain connection) before 300 cycles, as shown in Figure 5.22. Again the use of underfill improves the electrical continuity of the joint. This effect is more pronounced for the Pb-based solders than for the Pb- free solders. Up until 700 cycles, the failure rate is negligible but at 1000 cycles the failure noted for SnPb is 44 percent while that for SnAgCu is almost 100 percent. This can be seen in Figure 5.23. The performance of Pb-based solders is much better than the Pb-free solders. This is because Pb-free solders contain more Sn than Pb-free solders. This allows the Au from the ENIG surface finish to diffuse through the Sn matrix and reach the UBM side. Here it can interact with the Sn and form the brittle $AuSn_4$ as has been reported previously [Theuss et al. , 2003].

Since Pb-free solders also contain Cu, hence other complex ternary CuSnAu phases are also formed. In turn , these ternary phases consume the Ni out of Ni(V) barrier layer of the UBM forming new ternary and quaternary Sn-NiCu-(Au) IMC's. As a consequence, the UBM becomes dysfunctional and now uncontrolled diffusion of metals into the Silicon and vise versa can occur, thus the joint integrity is lost. This explains the poor electrical continuity observed for SnAgCu solder alloys during thermal shock.

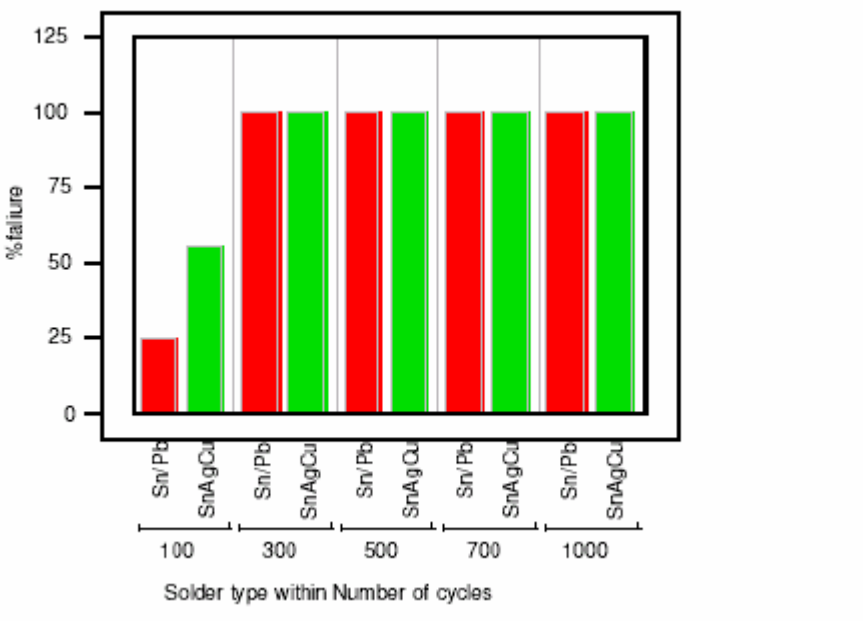


Figure 5.22 Electrical continuity without underfill (Thermal shock)

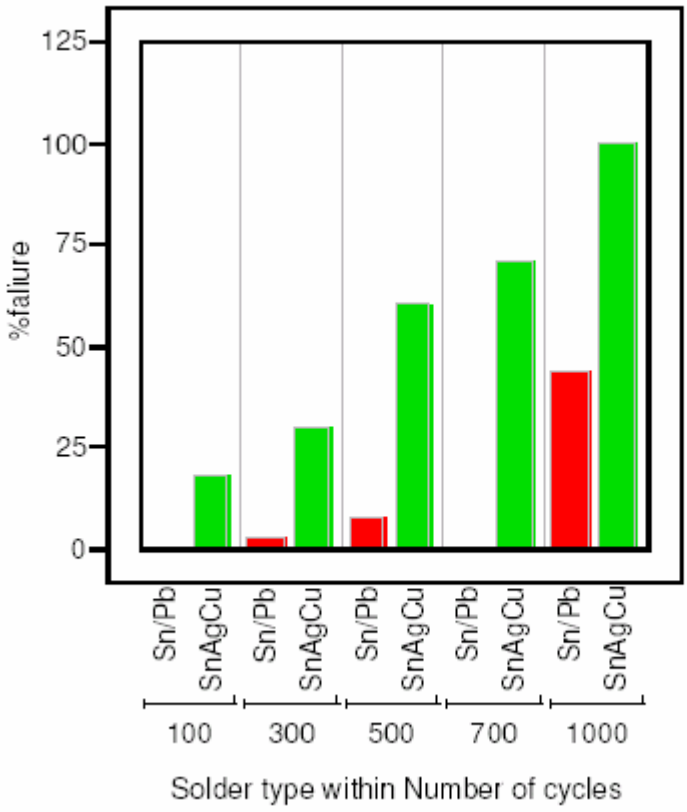


Figure 5.23 Electrical continuity with underfill (Thermal shock)

5.4.4 Discussion

The two solders differ much in their thermo-mechanical-electrical performance. This can be related to the IMC formation and growth. Just after reflow a thicker layer of IMC is formed in Sn-Ag-Cu which explains its high ball shear strength. But after 100 hrs of HTS Ag_3Sn and Cu-V-Sn intermetallics start forming which can cause reduced ball shear strength. Also needle shaped Ag_3Sn acts as stress concentrator and hence can cause an electrical open in Sn-Ag-Cu. In addition brittle compounds like $AuSn_4$ and other ternary compounds start forming which makes the UBM dysfunctional and uncontrolled

diffusion of metals takes place. This effect is more pronounced in thermal shock and hence we see a poor electrical performance of Sn-Ag-Cu. On the contrary, in Sn-Pb solders since less Sn is present, no brittle IMC's like Ag_3Sn, $AuSn_4$, and Cu-V-Sn are seen. Hence it shows consistent BS values across HTS hours.

On the substrate pad side, the ENIG pad finish shows the crack growth at the corner of the Ni-Cu pad interface. Ni of the ENIG contains phosphorous, which forms brittle compounds at higher storage hours. The cracking is not only because of the brittle nature of the phosphorus but also because of high inherent CTE difference between Ni and the Cu interface which leads to higher interfacial stresses as the modeling results in Chapter 4 suggested. Overall we see an improvement in the reliability with the underfill, as expected. This is because undefill redistributes the stresses.

5.5 Pb-free solder and UBM thickness: Experiment 2

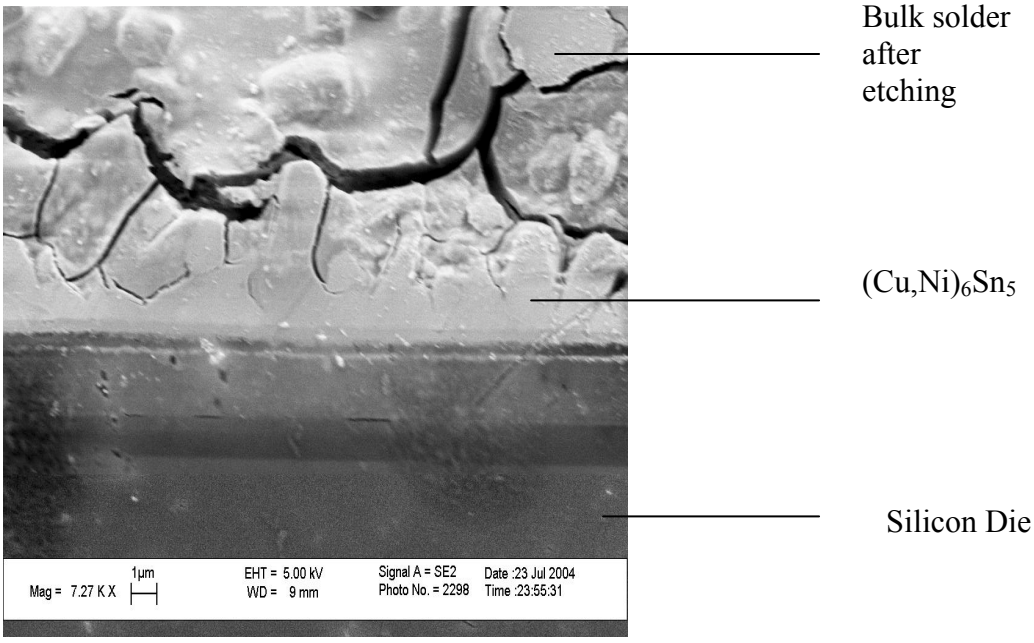
Results of Experiment 1 and modeling in Chapter 4 indicate that for lead-free solder on the UBM side a thicker layer of initial IMC is formed which is believed to be causing higher shear strength. In order to verify this, we do an experiment where the UBM wetting layer thicknesses are varied in order to get a different IMC thickness.

The three UBM wetting layer (Cu) thicknesses are 0.6 micron, 1 micron, and 1.2 micron. The FA-10 dies have Pb-free solder bumps. They are assembled as is described in Section 5.3.2 for Pb-free reflow conditions. Subsequently they are HTS tested upto 500 hrs.

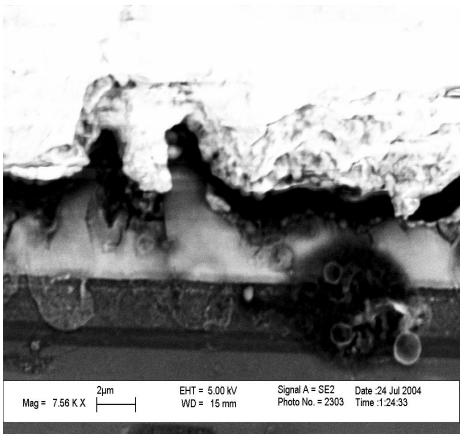
5.1 Intermetallic formation

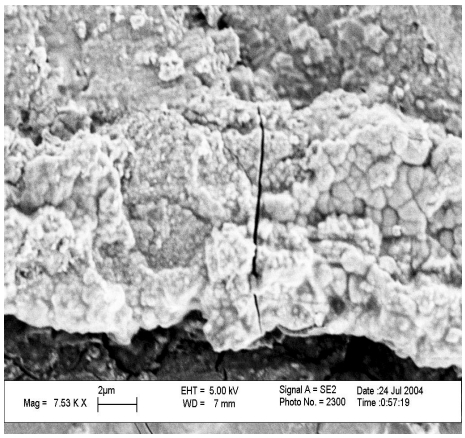
Comparison across different UBM thickness

The initial IMC formation thickness depends on the Cu wetting layer thickness to a certain extent. Thus a 1.2 µm layer thick Cu UBM layer would create a 1.2µm thick IMC layer. The layer is not continuous but it is a good approximation. This is seen in Figure 5.24 (a). As the wetting layer thickness decreases, the initial IMC formation also decreases. As the thickness is reduced to 0.6µm, it becomes increasingly difficult to distinguish the IMC layer. In Figure 5.24(a) the IMC is 1.2 micron thick and hence can be seen but in Figure 5.24(c) where the thickness reduces to 0.6µm the distinction decreases. This information has been used to model the fine pitch solder joint, as has been described in Chapter 4.



(a)



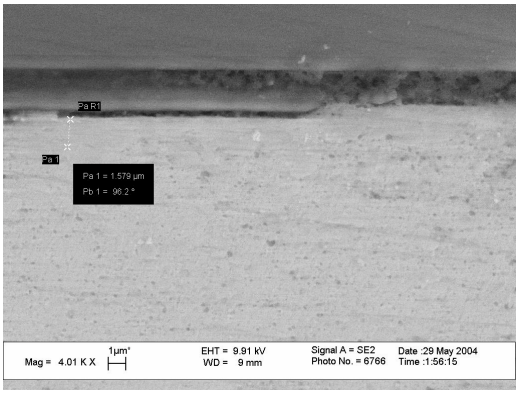


(b) (c)

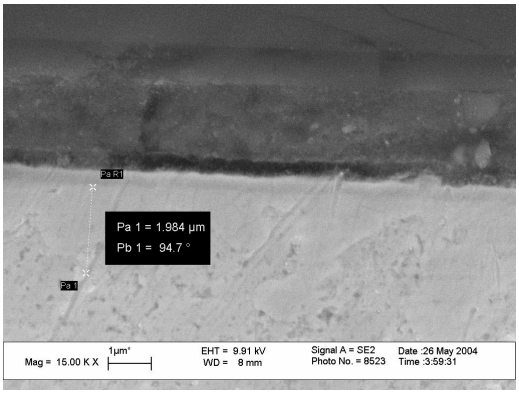
Figure 5.24 IMC formation after reflow (a) initial UBM wetting (Cu) is 1.2 µm (b) Initial UBM-Cu is 1.0 µm (c) Initial UBM-Cu is 0.6 µm

Rate of IMC formation

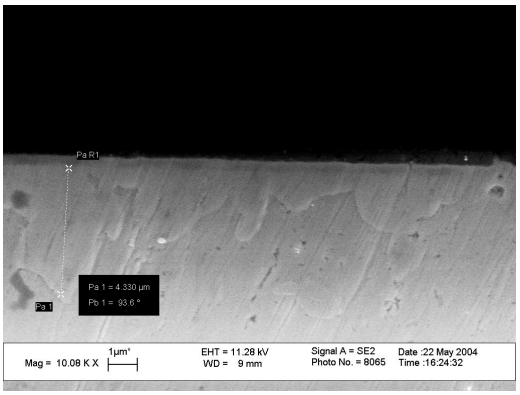
As thermal aging continues the IMC thickness increases due to diffusion and growth. Figure 5.25 shows increasing IMC thickness with thermal aging. The variation in the IMC layer can be high after 350 hrs of HTS, with the minimum and the maximum thickness showing considerable difference. In that case an average values is taken. Table 5.5 shows the average value of the IMC thickness taken at different times. The square of the plot is almost a straight line as is seen in Figure 5.26. This indicates parabolic rate of growth. Hence we calculate the rate constant of the IMC formation from the slope of the graph as K = 0.0176 μm^2/ hrs.



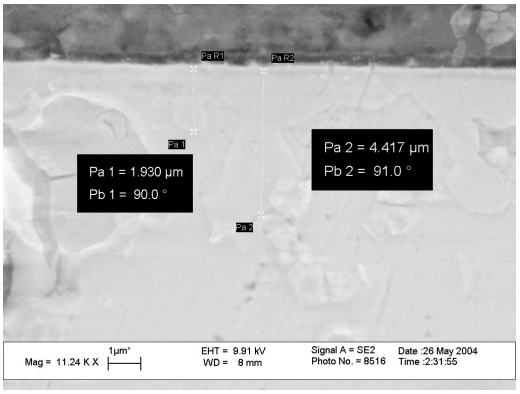
(a) 100 hrs HTS



(b) 200hrs HTS



(c) 350 hrs HTS



(d) 500 hrs HTS

Figure 5.25 IMC formation as HTS aging

Table 5.5 UBM_IMC thickness as aging at 150 °C

HTS Hours	**Average IMC thickness (µm)**	**IMC thickness square (μm^2)**
0	0.6	0.36
100	1.579	2.493241
200	1.984	3.936256
350	2.7	7.29
500	3	9

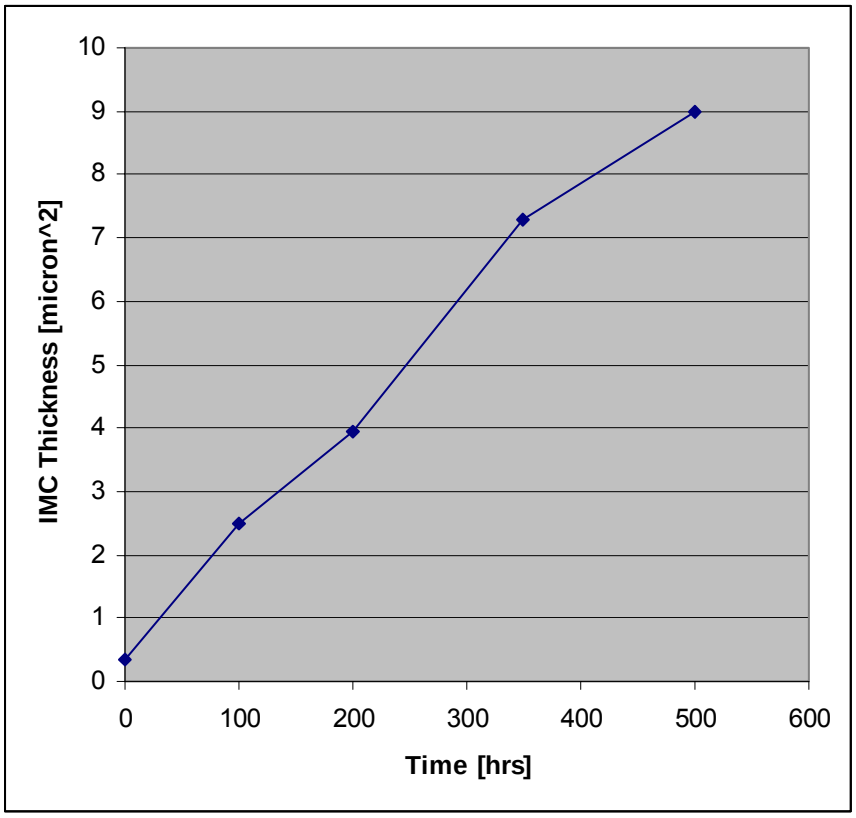


Figure 5.26 Plot of IMC thickness square vs time

5.5.2 Mechanical/Electrical strength

The die shear results across different UBM thicknesses and HTS hours do not vary significantly. In contrast we see a marked difference in the ball shear values for different UBM thicknesses. Electrical continuity also shows no variation with changing UBM thickness.

5.5.3 Discussion

Since the initially formed IMC thickness governs the BS values, hence thicker the IMC layer, higher is the ball shear strength. In contrast, in die shear the fracture occurs in the

bulk of solder. Hence the UBM thickness or IMC growth has no effect. Similarly, since the IMC primarily affecting the electrical continuity, Ag_3Sn forms in the bulk of solder. Hence UBM thickness has no effect on the electrical continuity.

5.6 Evaluation of different substrate pad finishes/ top surface metallurgies: Experiment 3

Section 5.4.1 shows that the ENIG pad finish causes the cracks at the Ni-Cu interface. We found out that one of the reasons for these cracks is the formation of the brittle P compound formed at the interface. But the modeling results in Section 4.1.2 proved that even if P brittle compounds are not present the Ni-Cu pad interface is highly stressed. Ni has a lower CTE of 13.1 ppm; as compared to solder (CTE of 22 ppm) and Cu (CTE of 17 ppm). Thus there is a higher CTE mismatch. This suggests that pad finish devoid of Ni would result in (a) lesser interfacial stresses; (b) no phosphorous, as phosphorous is deposited during Ni deposition. Hence we use direct surface pad finishes, with only Cu as the underlying layer and hence the CTE mismatch is less. In this research we chose three different substrate pad finishes as possible alternatives. The different surface pad finishes studied are:

1. OSP (0.2-0.5 μm)
2. Direct Gold (0.08-0.15 μm)
3. Direct silver (0.3-0.6 μm)

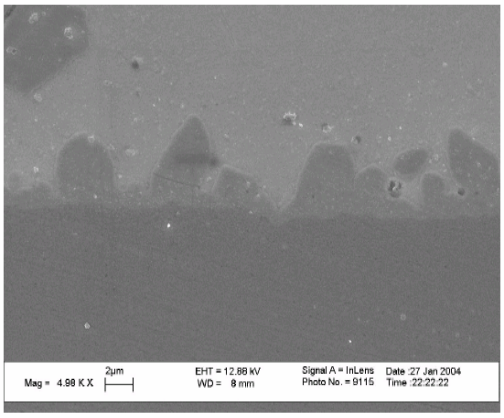
Different substrate pad coupons were screen printed with Sn95.5-Ag3.8-Cu0.7 solder using 0.002 inch thick stencil with a snap of height 0.02 inches. These were then passed through the reflow oven, thermally aged and ball shear strengths evaluated. The reflow conditions are same as in Figure 5.6. The aging and the BS conditions are

described in Section 5.3.2. FA10 dies were assembled on these three pad finishes and then die shear tested.

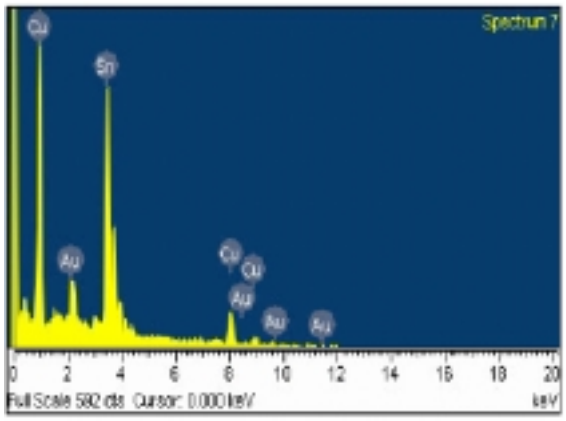
5.6.1 Intermetallic formation

Comparison of IMC formation in the three pad finish provides some understanding into the various pad finishes. Silver is not detected in direct immersion silver/Cu pad interface. On the contrary gold is detected in the direct immersion gold IMC. This indicates that silver wets the solder better then the gold surface pad finish. The percentage of Sn detected in OSP is less than that detected in the other two systems.

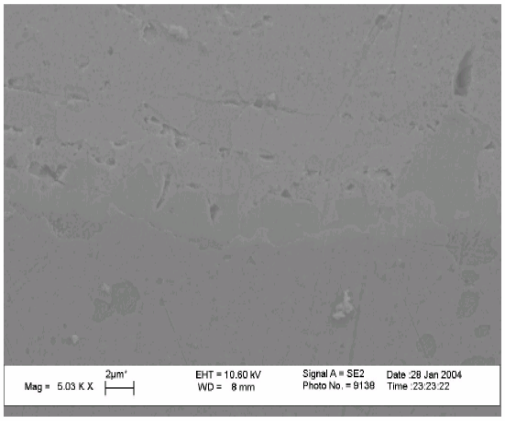
The shape of the IMC formed is scallop in both the metal based finishes. But, the IMC is more continuous in the OSP surface pad finishes. Figure 5.27 shows the various IMC's formed.



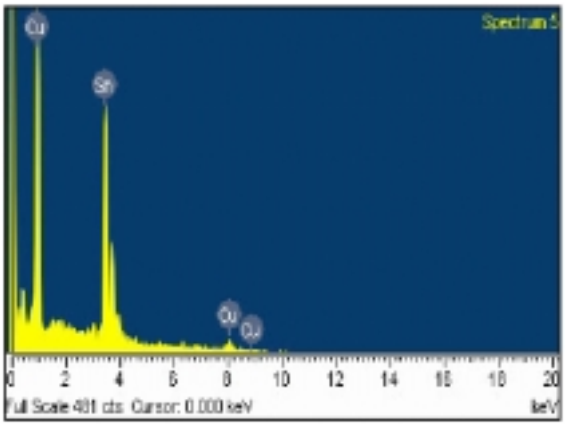
(a) Direct Immersion Gold-SnAgCu



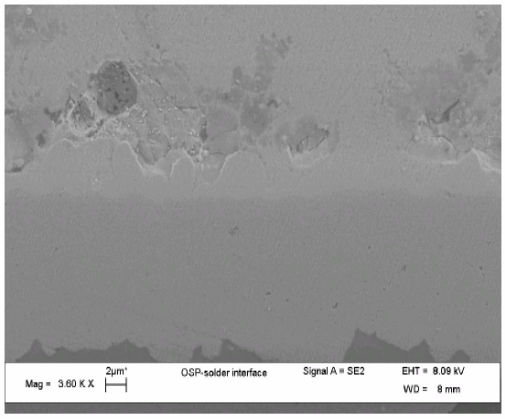
(b) EDX of IMC



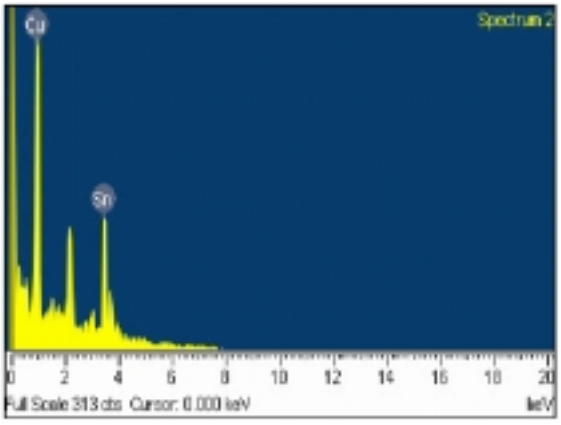
(c) Direct Immersion Silver-SnAgCu



(d) EDX of IMC



(e) OSP-SnAgCu interface.



(f) EDX of IMC

Figure 5.27 IMC formation in as reflowed substrate pad finishes

5.6.2 Mechanical strength

Ball shear results

SnAgCu stencil printed and reflowed substrates were kept at 150 ºC for 100 hr. Subsequently the ball shear values were measured. As reflowed, direct immersion silver substrate shows the maximum ball shear strength, among the three. Figure 5.28 plots the ball shear values vs. different pad finishes. Note that all three substrate pad finishes show

reduction in ball shear after 100 hrs HTS testing. Figure 5.29 confirms that the silver pad finish shows the maximum ball shear values even after 100 hrs of HTS testing.

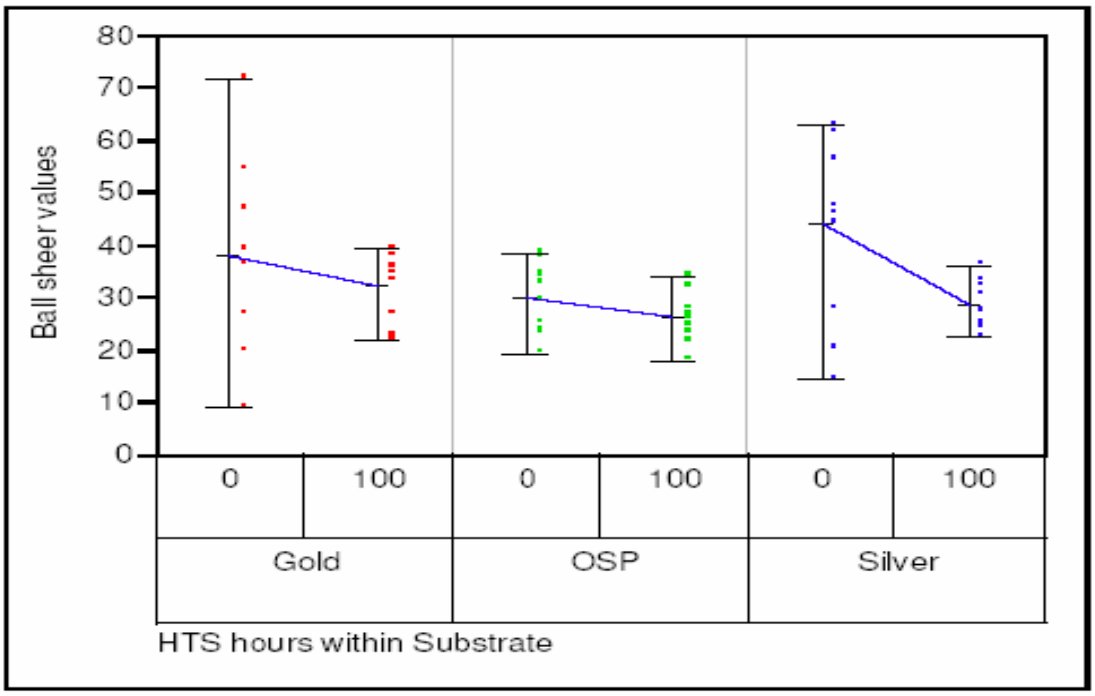


Figure 5.28 Ball shear for different substrate pad finishes: showing effect of HTS on each of the surface pad finishes.

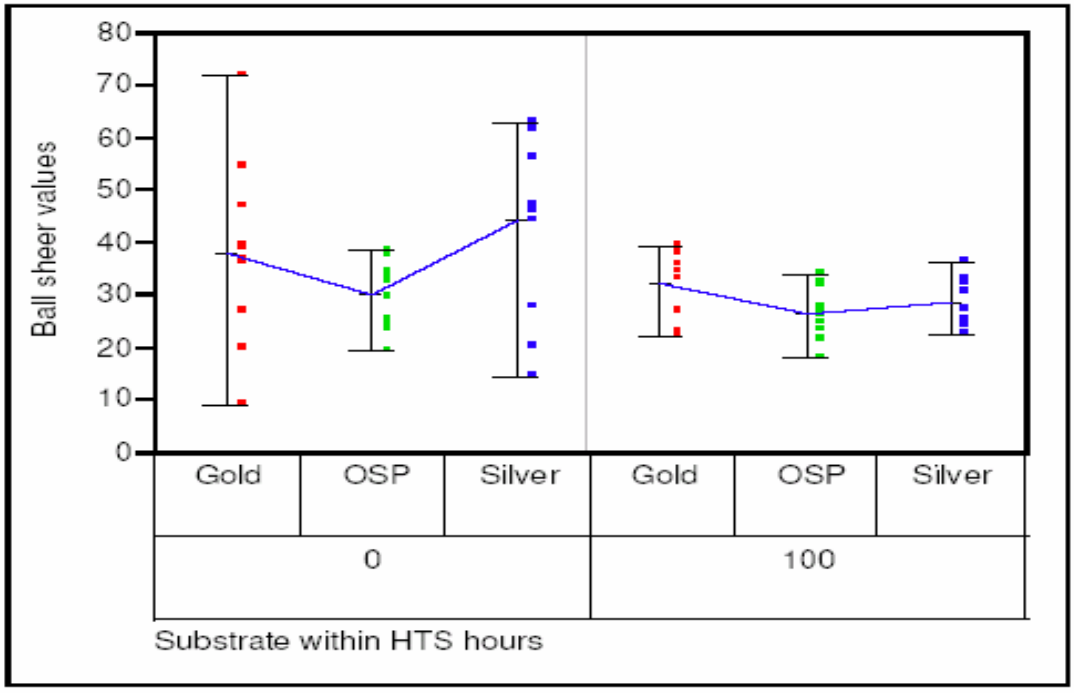


Figure 5.29 Ball shear for different substrate pad finishes: analyzing behavior among pad finishes.

Assembly of the FA10

The assembly of the pad finishes is a major concern. It requires multiple reflows in order to form a solder joint. Use of nitrogen helps in reducing non-wets but nevertheless assembly yield is less compared to ENIG.

Die shear

The die shear strengths of as reflowed direct gold, OSP and direct silver are comparable and statistically show no difference. The values decrease by as much as 13 percent after 100 hrs HTS. This is shown in Figure 5.31. The fracture during the die shear does not occur at the solder-pad interface which shows that the IMC formation is strong for these surface pads. A typical die shear picture for these pad finishes is shown in Figure 5.30. This SEM picture was taken after die shear of the silver surface after 100 hrs

HTS. Note that the solder still remains on each of the surfaces indicating surface pad with good mechanical strength. The bright part is the left over flux.

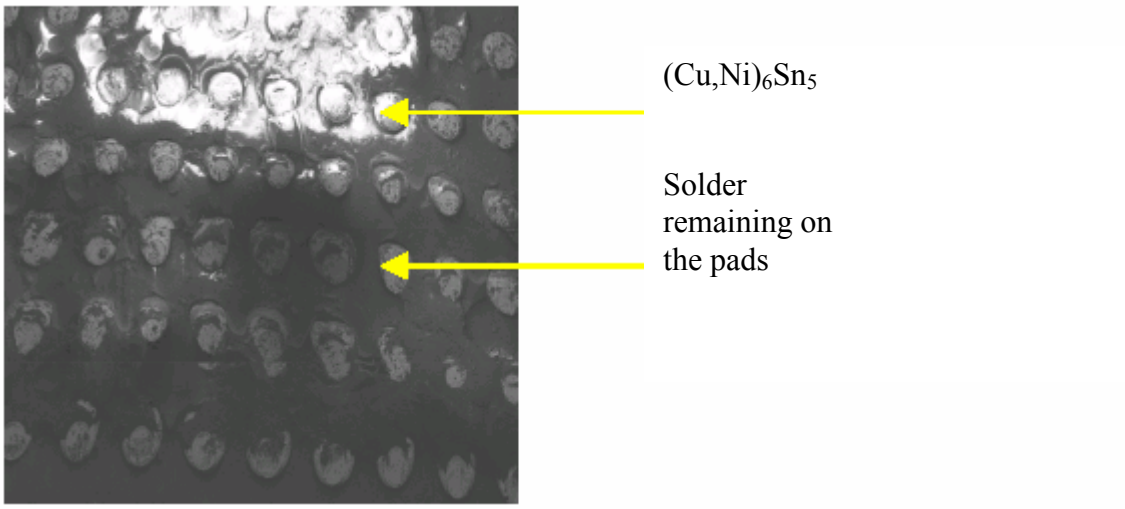


Figure 5.30. SEM of silver pad die shear

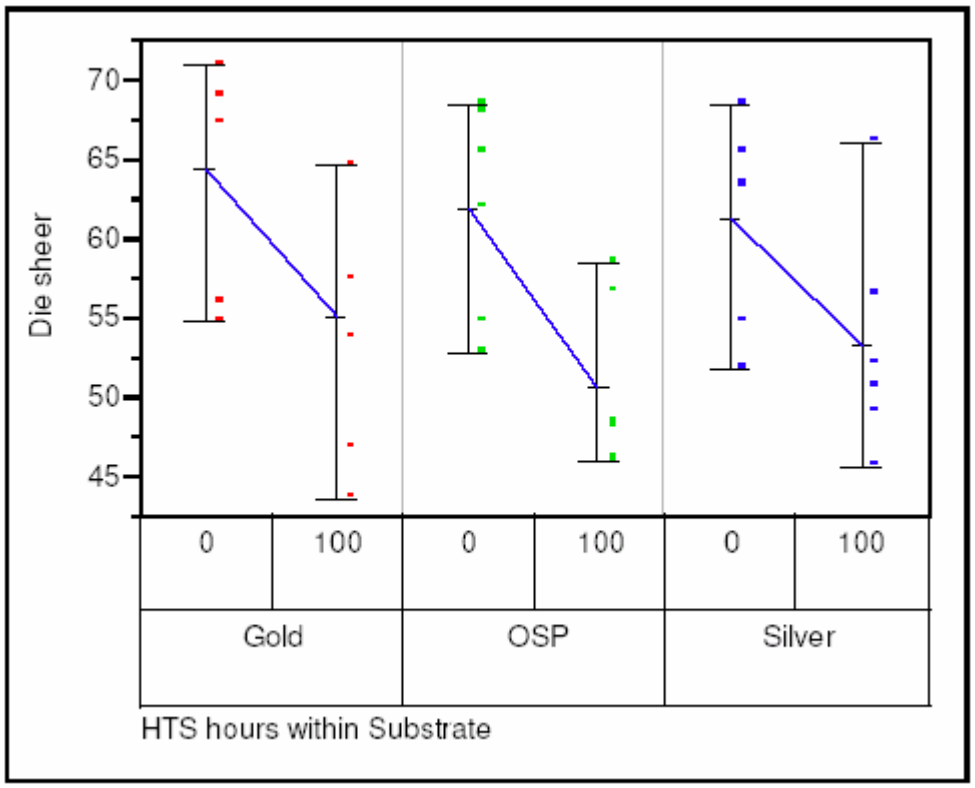


Figure 5.31 Die shear for different substrate pad finishes.

5.6.3 Electrical continuity

The electrical resistance of direct gold and immersion silver is almost the same as that of ENIG pad finishes. But OSP shows considerably higher electrical resistance [Gupta et al., 2004]. A major concern with all these three surface pad finishes is the wetting of the solder on these surface pad finishes. All of them require multiple reflows (2-3) times, in order for the electrically-conductive solder joint to form.

5.6.4 Discussion

The IMC results indicate that the coating is uniform for all the three substrate pad finishes. And silver shows good wetting with the Sn-Ag-Cu solder. The assembly conditions are very stringent for all the pad finishes; with direct gold requiring the tightest controls.

5.7 Summary

Three separate experiments were carried out in order to evaluate solder, IMC thickness and TSM effects on the flip–chip thermo-mechanical-electrical reliability. Ag_3Sn and Cu_6Sn_5 are the critical IMC's formed. These affect the reliability. The UBM thickness is found to have an effect on the mechanical strength as well. Among the three pad finishes, preliminary results of direct immersion silver are promising. Assembly of these new pad finishes remains a major concern.

CHAPTER 6

SUMMARY AND FUTURE WORK

This chapter summarizes the research work. Suggestions are made for future work to remove other bottlenecks towards achieving next generation lead-free fine pitch flip-chip packaging goals.

6.1 Summary

In this research effect of intermetallic compounds on thermo-mechanical reliability of lead-free solder interconnects for flip-chips have been discussed. FEA modeling is carried out to predict the stresses at various interfaces in the flip-chip on board package during thermo-mechanical loading. The time and temperature dependent deformation accumulates with repeated cycling and ultimately causes delamination, solder joint cracking or interconnect failure. Effects of IMC thickness on the delamination have been discussed. The critical interfaces identified via modeling are intermetallic/UBM system, and substrate pad/solder interfaces. Thus the three important material parameters identified are the i. solder, ii. UBM and iii. substrate pad finish. These affect the IMC formation and growth. Hence experiments are designed in order to understand role of these parameters in the FCOB reliability.

In the first experiment, the two solders compared are eutectic Pb solder and Pb-free solder. These two differ in their thermo-mechanical-electrical performance. This can be related to the IMC formation and growth.

Experiment 2 is a validation of FEM modeling as well as Experiment 1 results. It tries to correlates the UBM wetting layer thickness to the initial IMC formation. Hence in order to verify this we carry an experiment where the UBM wetting layer thicknesses are varied in order to get a different IMC thickness.

The third parameter studied is the substrate pad finish. IMC formation results indicate that the coating is uniform for all the three substrate pad finishes. And direct silver shows better wetting as compared to direct gold with the Sn-Ag-Cu solder. Stringent assembly conditions are required; sometimes requiring as much as 2-3 reflows in order to form an electrical connection.

In a nut shell following conclusions emerge from the research:

- Pb-free solders show higher mechanical strength as compared to Pb-based solders due to thicker IMC layers.
- Pb-free solders show poor electrical performance due to Ag_3Sn intermetallic.
- FEM modeling and experimental results shows that thicker the IMC layer, lesser is the delamination.
- FEM modeling shows that thicker the UBM side intermetallic, slower is the fatigue initiation.
- ENIG pad finish shows cracks with Pb-free solder as aging continues.

- Direct immersion silver looks best as a replacement for ENIG; provided assembly is strictly controlled.

6.2 Future Work

This research characterized a number of aspects of the reliability as affected by the intermetallics in Pb-free systems. There are other aspects that need to be addressed before Pb-free flip-chip reliability standards can be quantified. Some suggested future work are as follows:

- Incorporate the visco-elastic material properties of Pb-free solder in modeling.
- The analytical equations for delamination need to be modified to account for the 3-D modeling.
- Use the developed FEM model to vary the substrate pad finishes.
- A time dependent experimental study of IMC formation is required for different pad finishes.
- More rigorous measurements of stress in dielectric film and silicon die to establish the techniques introduced in this work.

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